Part I

Simulate the common emitter amplifier that was designed in Problem D4.82 using PSpice. For the BJT, use the 2N2222 transistor model provided in the PSpice library ($\beta=255$). Set the "infinite" capacitors at a value of 10 $\mu$F, and choose an amplitude for $v_s$ that is sufficiently low that the output is not distorted.

a) What is the voltage gain of the amplifier? Why is the gain larger than the answer to Problem D4.82?

b) Using "AC sweep" in the Analysis/Setup menu, determine the lower and upper cutoff frequencies. Remember, these are the frequencies at which the gain drops by 3 dB (or a factor of 0.707) from the mid-frequency gain.

Part II

A new application for the amplifier in Part I is to drive a 300$\Omega$ antenna. To model this antenna, you can replace $R_L$ in the circuit with a 300$\Omega$ resistance. Since the voltage gain for a CE amplifier is $A_V \approx -g_m(R_c||R_L||r_o)$, the gain will drop to a very small value due to the new 300$\Omega$ load.

a) Design a common collector amplifier to help drive the 300$\Omega$ antenna. The input to the CC amplifier should be the output of the CE amplifier in Problem D4.82 (without C and $R_L$). The output of the CC amplifier should be connected to the 300$\Omega$ antenna resistance through a coupling capacitor such that the DC part of the solution is blocked from the antenna.

b) What is the input resistance ($R_i$) of the CC amplifier stage? How does this compare to the original 50k$\Omega$ load resistance that was attached to the output of the CE amplifier? What will happen to the gain of the CE amplifier when the 50k$\Omega$ load is replaced by the input of the CC amplifier?

c) Modify the PSpice simulation from Part I to include your new CC amplifier. What is the gain of the entire 2-stage amplifier? ($A_v = \frac{v_{antenna}}{v_s}$)