Electronics
EECE2412 — Spring 2018
Exam #3

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File:12262/exams/exam2

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Name: _____

General Rules:

- You may make use of three sheets of notes, 8.5–by–11 inches, using both sides of the page.
- You may use a calculator.
- Present your work as clearly as possible. I give partial credit if I can figure out that you know what you are doing. I do not give credit for putting down everything you know and hoping I will find something correct in it.
- Each question has a vertical black bar providing space for your work and a line for numerical answers or box for plots or drawings. Please write your answer to each question clearly. If it happens to be correct, I give you points quickly and move on to the next problem. Please show your work in the space provided, or on extra pages, clearly labeled with the problem number. If the answer is wrong, this will make it easy for me to find ways to give you partial credit.
- Avoid any appearance of academic dishonesty. Do not talk to other students during the exam. Keep phones, computers, and other electronic devices other than calculators secured and out of reach.

1 Short–Answer Questions

1. Two MOSFETs have identical properties except that one has a larger channel width, W. That one will have larger K and will be capable of carrying more current.

   - [x] True
   - [ ] False

2. The gate current on an N–Channel MOSFET is

   - [ ] positive.
   - [ ] negative.
   - [x] zero.

3. Electrostatic precautions are more important working with BJTs than FETs.

   - [ ] True
   - [x] False

4. The threshold voltage V_{t0} for an enhancement NFET is positive.

   - [x] True
   - [ ] False

5. Positive V_{GS} on an N–Channel JFET will

   - [ ] increase the drain current.
   - [ ] decrease the drain current..
   - [x] destroy the transistor.

6. A common-drain amplifier is used for

   - [x] unit voltage gain.
   - [ ] unit current gain.

☐ high gain.

7. An FET amplifier can have a very high input impedance.

☒ True
☐ False

8. For an amplifier, the FET should be in saturation.

☒ True
☐ False

9. CMOS logic consumes power only when switching.

☒ True
☐ False

10. The switching speed of a CMOS logic gate is generally determined by the capacitance of the gates of the logic circuits that follow it.

☒ True
☐ False

2 FET DC Bias

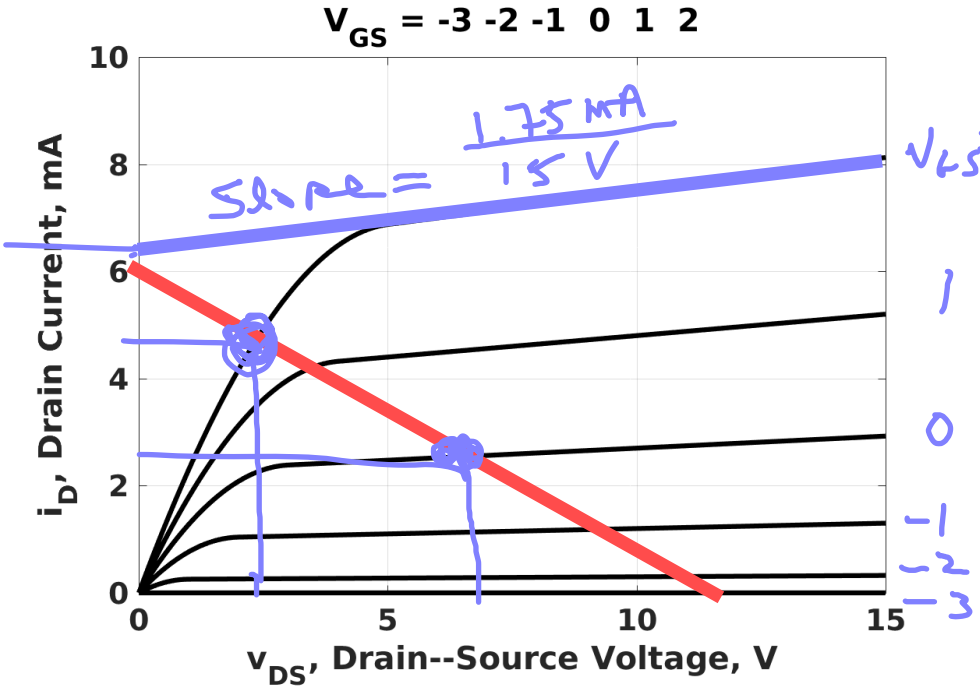
2.1 Reading the Curves

The figure shows a set of I–V curves for a particular NFET.
From the graph, determine the following (Assume $kp = 50\ \mu\text{A/V}^2$);

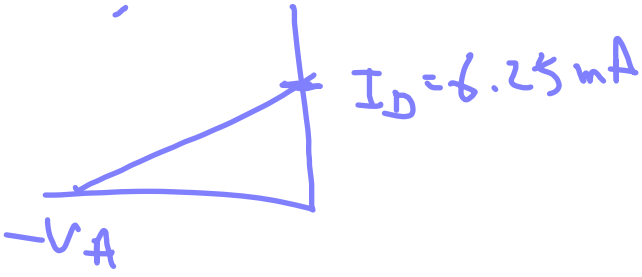
Threshold Voltage, $V_{t0} =$ −3 Volts

Width/Length Ratio, $W/L =$ 10

Approximate Early Voltage, $V_A =$ 54 (actual was 50) Volts



$$K = \frac{6.25\text{mA}}{(2-(-3))\text{ V}^2} = \frac{W}{L}\frac{kp}{2} \qquad \boxed{\frac{W}{L} = 10}$$

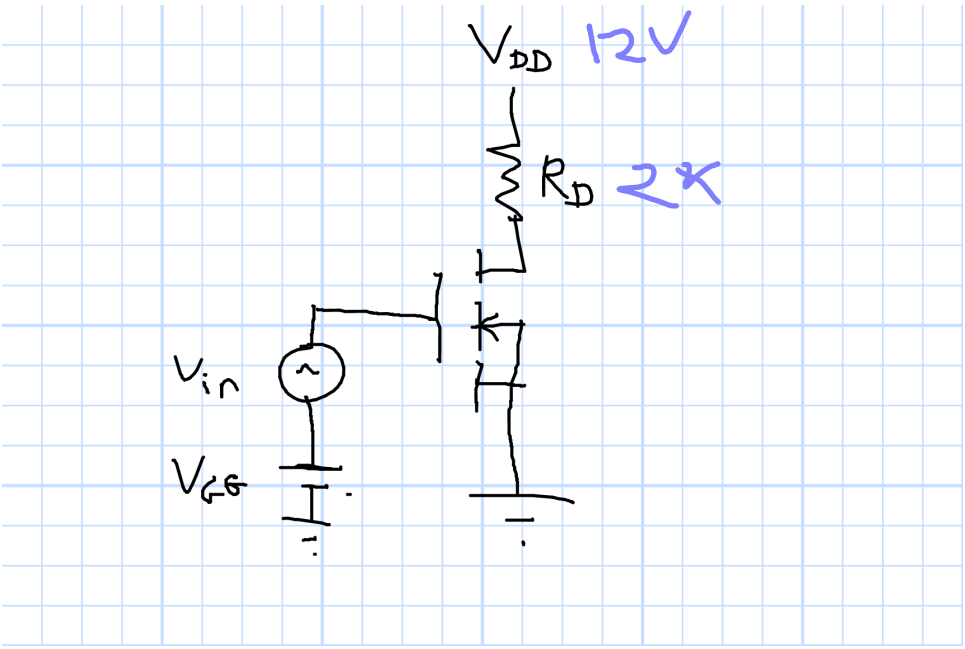


$$\text{Slope} = \frac{I_D}{V_A}$$

$$\frac{6.25\text{mA}}{V_A} = \frac{1.75\text{ mA}}{15\text{V}} \qquad \boxed{V_A = 54\text{ V}}$$

2.2 Load Line

The transistor is placed in the following circuit.



For two cases, draw the load lines on the figure and write the equations for calculating the DC drain current, I_D. Remember that you can neglect the Early effect at this point.

You do not need to solve the equations; just write them and estimate the answer graphically from the plot.

Case 1: $V_{GG} = 2$ V

Equation: $I_D = K(V_{GG} + 3V)^2$

Estimated Drain Current, $I_D =$ 5 mA.

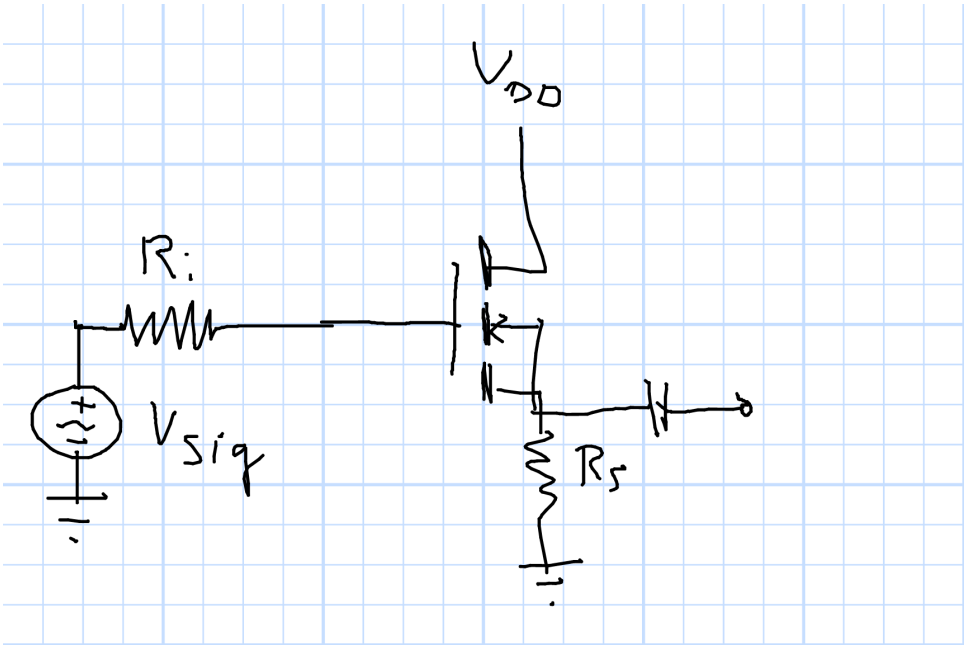
Case 2: $V_{GG} = 0$ V

Equation: $I_D = K[2(3)(12 - I_D * 2k) - (12 - I_D * 2k)^2]$

Estimated Drain Current, $I_D =$ 2.5 mA.

3 FET Amplifier

Consider the circuit shown. The transistor's Early voltage is $V_A = 50$ V, and the transistor is in saturation. In the circuit, the transconductance is $g_m = 2$ mA/V, the DC drain current is $I_D = 2$ mA, $R_i = 100$ kΩ, $R_S = 8$ kΩ, and the capacitor is "large enough."



3.1 Small Signal Parameters

What is W/L for this transistor? Remember $kp = 50$ μA/V^2.

$W/L =$ 20 .

What is r_d?

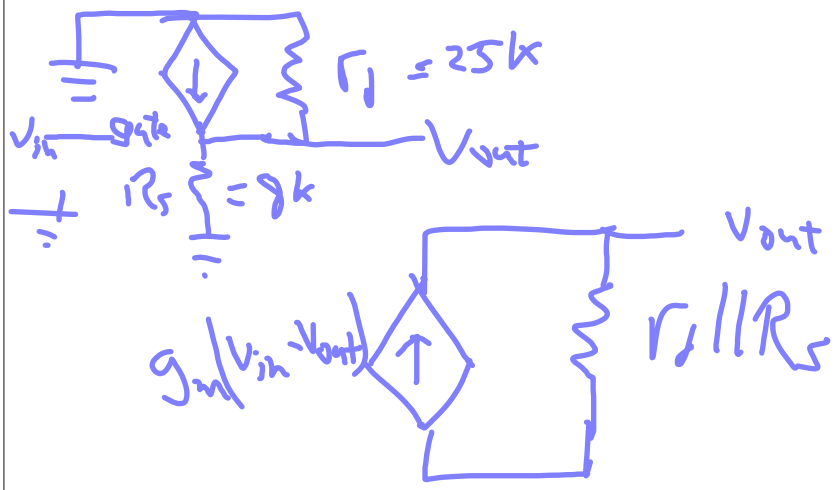
$r_d =$ 25 K Ω.

$g_m = 2\sqrt{kI_D}$ $\quad k = \left(\frac{g_m}{2}\right)^2 \frac{1}{I_D} = \frac{W}{L}\frac{kp}{2} = 1$

$r_d = \frac{50V}{2mA} = 25k$ $\quad \frac{W}{L} = \left(\frac{g_m}{2}\right)^2 \frac{2}{I_D k_p} = 20$

Draw the AC circuit.

(AC Circuit:)



3.2 Amplifier Parameters

$$V_{out} = g_m (V_{in} - V_{out}) \, r_d \| R_S$$

$$V_{out} \left[1 + g_m (r_d \| R_S) \right] = g_m V_{in} (r_d \| R_S)$$

$$\frac{V_{out}}{V_{in}} = \frac{g_m (r_d \| R_S)}{1 + g_m (r_d \| R_S)} = 0.92$$

$$r_d \| R_S = 6k$$

What is the voltage gain?

$A_V =$ 0.92 .

What is the input impedance?

$Z_{in} =$ ∞ Ohms. (no current in gate)

What is the output impedance?

$Z_{out} =$ 6 k Ohms.

3.3 Bonus Question

You do not need to answer this to score 100 on the exam. If you answer it correctly, I'll use the points in some way that will help your course grade.

What is the minimum voltage for V_{DD} to make this circuit work?

$V_{DD} =$ 18 Volts.

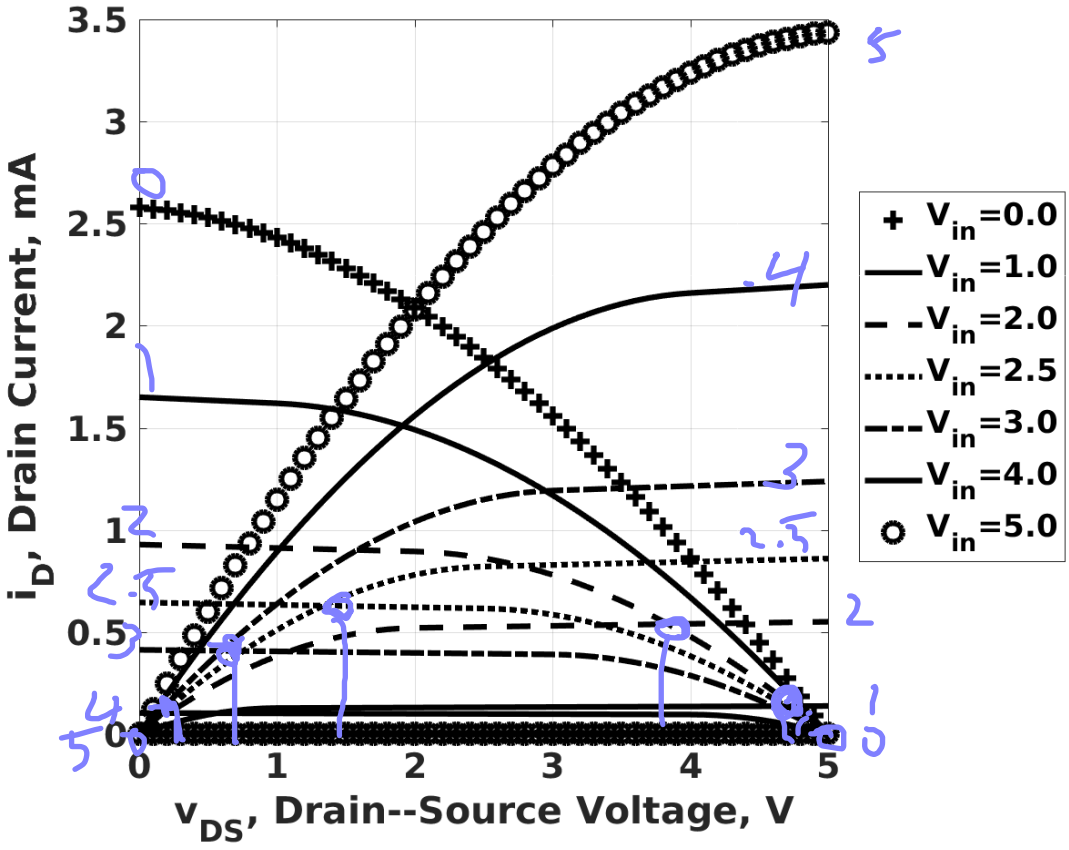
$V_S = 2\,mA \times 8\,k = 16\,V$

for saturation $V_{DS} > \sqrt{\frac{I_D}{k}} = \sqrt{\frac{2\,mA}{500\,uA/V^2}}$

$= 2\,V$

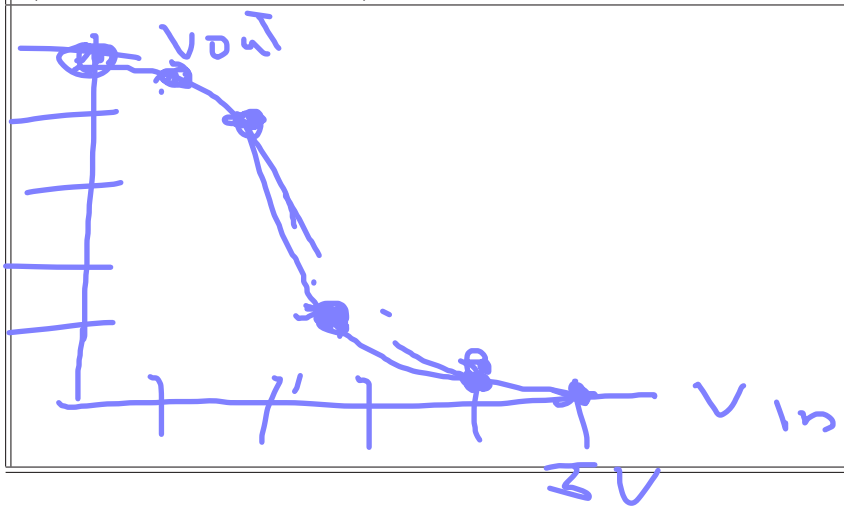
4 FET Logic

4.1 Transfer Function

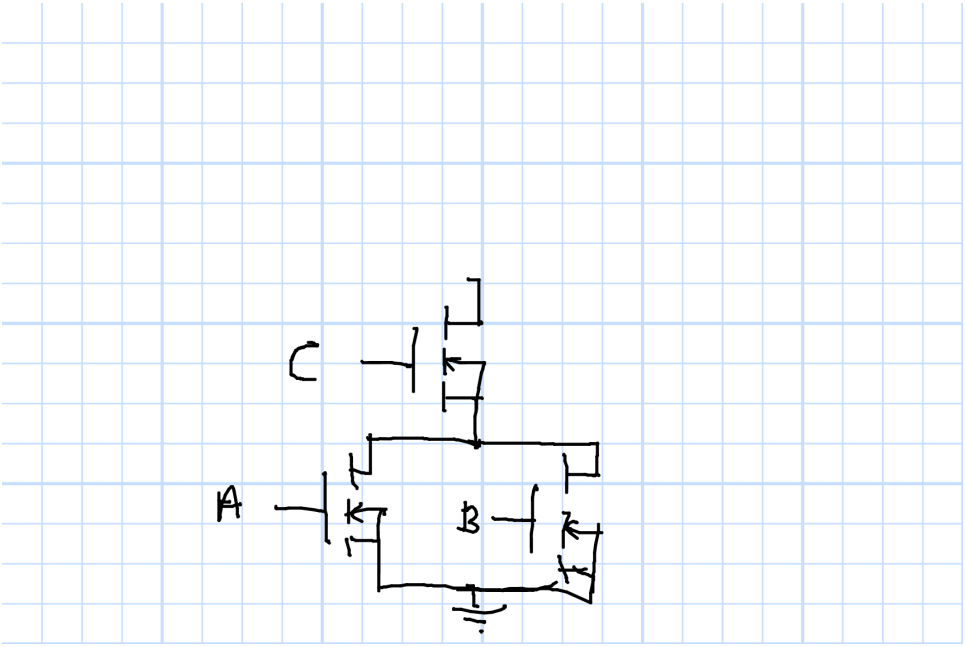


From the given transistor curves for a CMOS logic inverter in the figure above, draw the transfer function. Be sure to show numbers on the axes.

(Transfer Characteristic:)



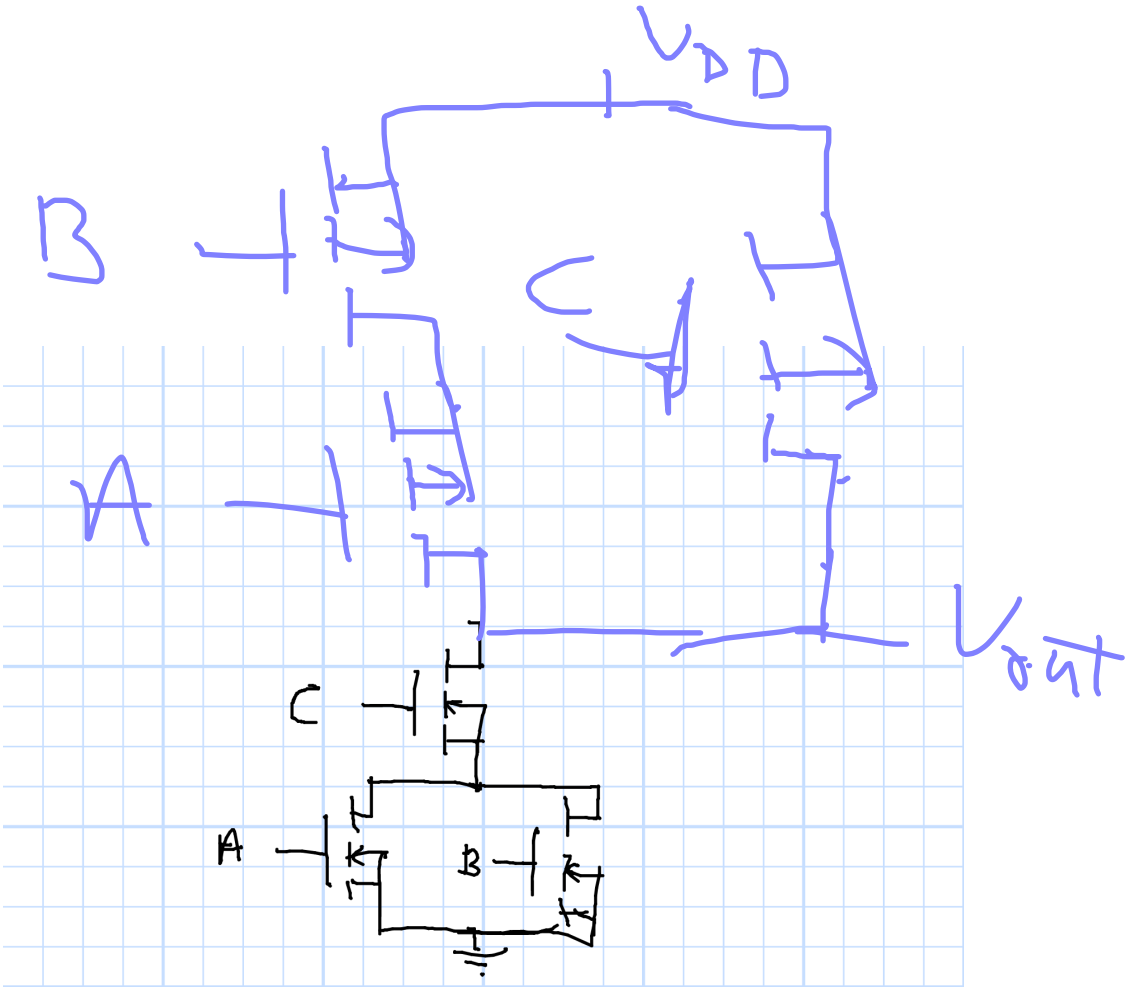
4.2 Logic Gate Design



The figure shows the pull–down portion of a logic gate with three inputs. For all possible combinations of true and false inputs, show show whether the pull–down circuit is open or shorted.

A	B	C	Open or Short?
0	0	0	open
0	0	1	open
0	1	0	open
0	1	1	short
1	0	0	open
1	0	1	short
1	1	0	open
1	1	1	short

Draw the corresponding pull–up portion on the diagram below.



What is the function of the resulting logic circuit?

Not [(A or B) and C]

$\overline{(A+B)C}$