

Electronics
EECE2412 — Spring 2017
Exam #3

Prof. Charles A. DiMarzio
Department of Electrical and Computer Engineering
Northeastern University

File:12198/exams/exam3

28 April 2017

Name: _____ :

General Rules:

- You may make use of two sheets of notes, 8.5-by-11 inches, using both sides of the page.
- You may use a calculator. Sharing of calculators is not allowed.
- Present your work as clearly as possible. I give partial credit if I can figure out that you know what you are doing. I do not give credit for putting down everything you know and hoping I will find something correct in it.
- Each question has a vertical black bar providing space for your work and a line for numerical answers. Please write your answer to each question clearly. If it happens to be correct, I give you points quickly and move on to the next problem. Please show your work in the space provided, or on extra pages, clearly labeled with the problem number. If the answer is wrong, this will make it easy for me to find ways to give you partial credit.
- Avoid any appearance of academic dishonesty. Do not talk to other students during the exam. Keep phones, computers, and other electronic devices other than calculators secured and out of reach.

1 Short-Answer Questions (33%)

A common-gate amplifier typically has a voltage gain of 1. ...

True False

Amplifiers built with FETs usually have high input impedance. ...

True False

CMOS logic circuits only consume power during transition between states.

True False

How is a depletion FET different from an enhancement FET? ...

Why is there no gate current in an FET? ...

What happens if the gate on an N-Channel JFET is more positive than the source?

An FET is very sensitive to electrostatic discharge. ...

True False

We want to design a PFET with the same K as an NFET. What parameter of the design can we change to make this happen?

If we use an FET as an active load, what is the important parameter?

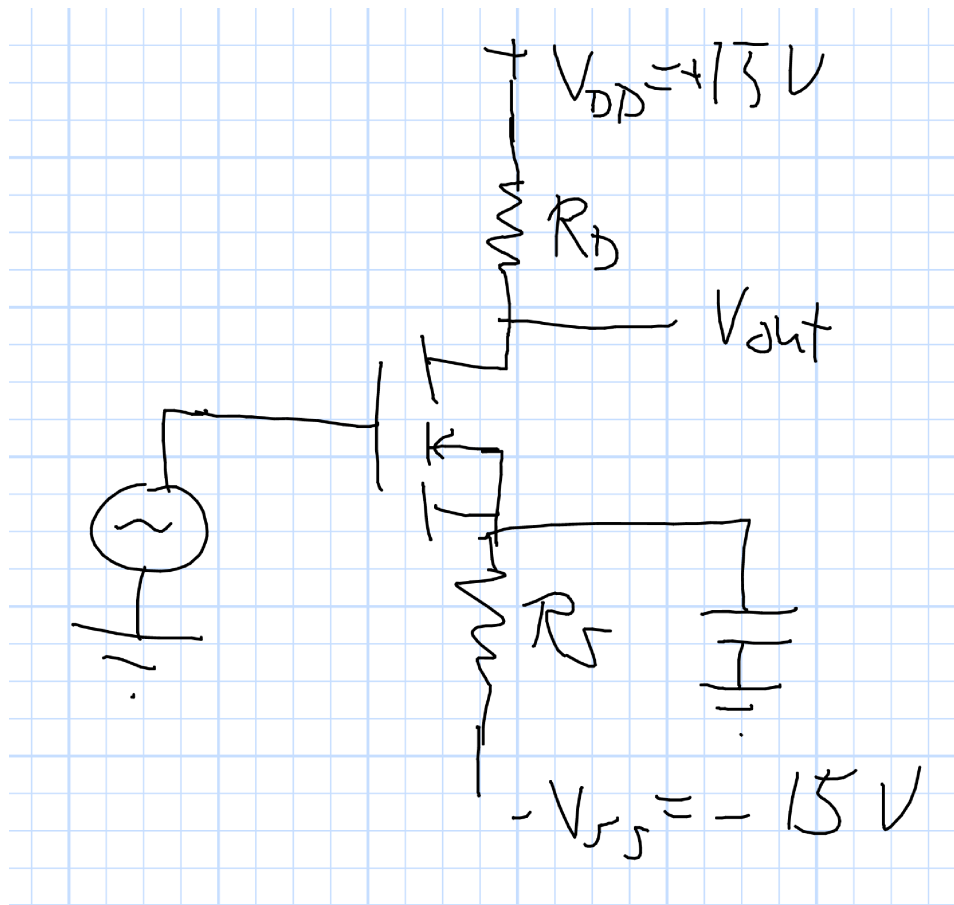
r_0 , K , r_{on}

In a current-mirror circuit, the mirror transistor is in triode mode. ...

True False

2 FET Amplifier (33%)

Consider the amplifier in the figure below. Some of the transistor specifications are $KP = 50 \mu\text{A}/\text{V}^2$, $V_{T0} = 2 \text{ V}$, and $V_A = 100 \text{ V}$.



2.1 DC Analysis

We want $I_D = 1 \text{ mA}$ and we want the voltage at the transistor's source to be -4 V , and we want V_{DS} to be one third of the total voltage across R_D , the transistor, and R_S . Determine the necessary W/L ratio for the transistor. Also, determine R_S and R_C .

$$W/L = \underline{\hspace{10em}} .$$

$$R_S = \underline{\hspace{10em}} \text{ Ohms.}$$

$$R_D = \underline{\hspace{10em}} \text{ Ohms.}$$

2.2 Small-Signal Parameters

Determine the transconductance, g_m , and the drain-source resistor, r_0 .

$$g_m = \underline{\hspace{10em}} \text{ A/V.}$$

$$r_0 = \underline{\hspace{10em}} \text{ Ohms.}$$

2.3 AC Circuit and Amplifier

Draw the AC circuit and determine the voltage gain, A_V , input impedance, Z_{in} and output impedance, Z_{out} .

AC Circuit:

$$A_v = \underline{\hspace{2cm}} .$$

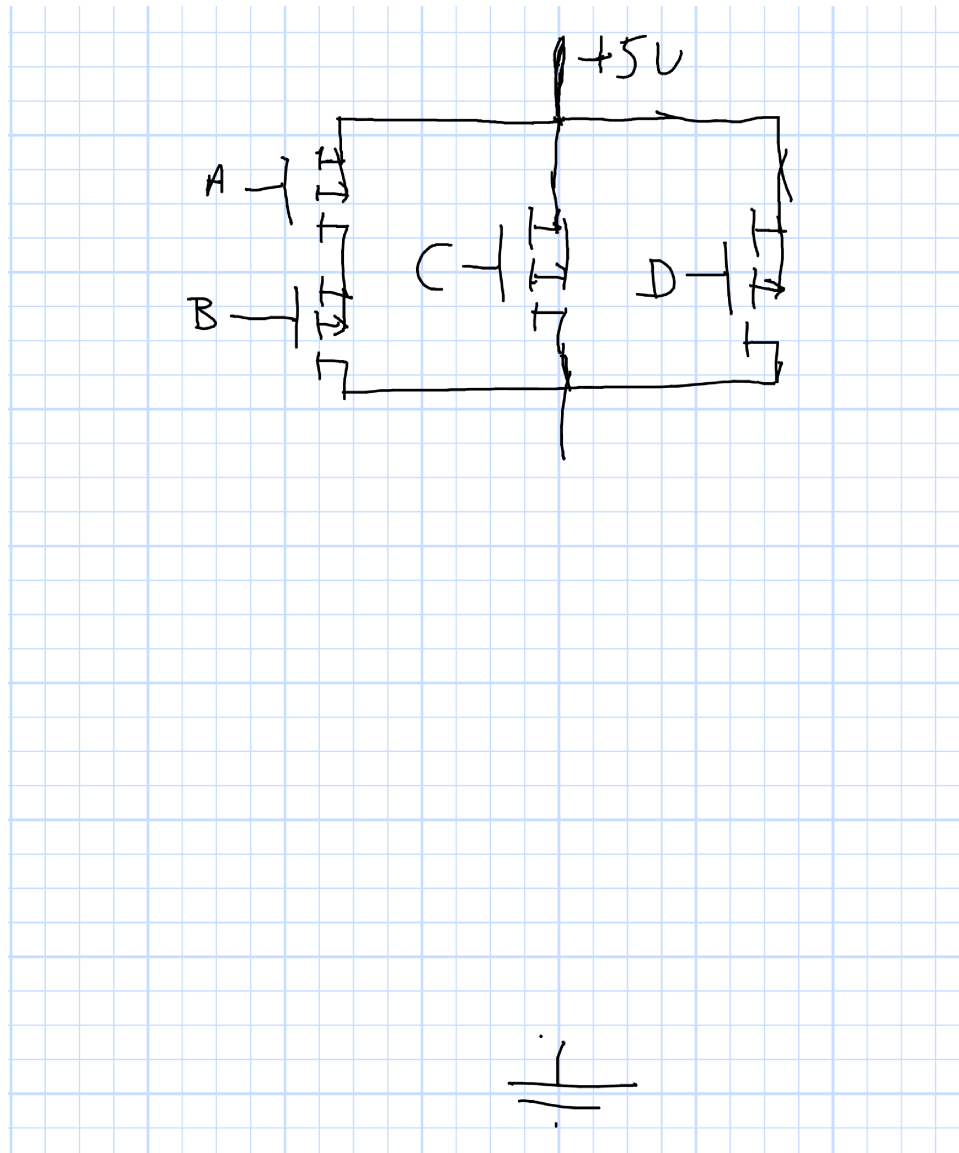
$$Z_{in} = \underline{\hspace{2cm}} \text{ Ohms.}$$

$$Z_{out} = \underline{\hspace{2cm}} \text{ Ohms.}$$

3 CMOS Logic (33%)

3.1 Circuit

Complete the logic circuit shown below.



3.2 Function

Complete the logic table for this circuit.

Logic Table: