Electronics
EECE2412 — Fall 2018
Exam #3

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Name: _____

General Rules:

- You may make use of three sheets of notes, 8.5–by–11 inches, using both sides of the page.
- You may use a calculator.
- Present your work as clearly as possible. I give partial credit if I can figure out that you know what you are doing. I do not give credit for putting down everything you know and hoping I will find something correct in it.
- Each question has a vertical black bar providing space for your work and a line for numerical answers or box for plots or drawings. Please write your answer to each question clearly. If it happens to be correct, and the work leading to it looks right, I give you points quickly and move on to the next problem. Please show your work in the space provided, or on extra pages, clearly labeled with the problem number. If the answer is wrong, this will make it easy for me to find ways to give you partial credit.
- Avoid any appearance of academic dishonesty. Do not talk to other students during the exam. Keep phones, computers, and other electronic devices other than calculators secured and out of reach.

1 Short–Answer Questions

In a field–effect transistor, the gate current is zero

☒ True ☐ False

For an N–Channel MOSFET, kp is typically ...

☒ 50 μA/V^2
☐ 500 μA/V^2
☐ 5 mA/V^2
☐ 50 mA/V^2

The gate–source voltage for an N–Channel JFET can only be negative.

☒ True ☐ False

In a CMOS circuit, for the PFET and NFET to have the same K, the ratio W/L should be the same for both transistors.

☐ True ☒ False

Pick the one most correct answer; An FET preamplifier would be useful in a capacitive microphone because of its ...

☒ High input impedance
☐ High gain
☐ Low Power Consumption

A common–drain amplifier is useful for its

☒ unit voltage gain
☐ unit current gain
☐ high gain

A CMOS logic circuit consumes power only when it is in transition from one state to the other.

☒ True ☐ False

CMOS logic can consist of only two–input NAND gates.

☒ True ☐ False

As the width, W, of the channel increases ...

☐ The frequency response goes up and the current carrying capacity goes up

☒ The frequency response goes down and the current carrying capacity goes up

☐ The frequency response goes up and the current carrying capacity goes up

☐ The frequency response goes down and the current carrying capacity goes down

Higher DC current, I_D, usually leads to higher amplifier gain

☒ True ☐ False

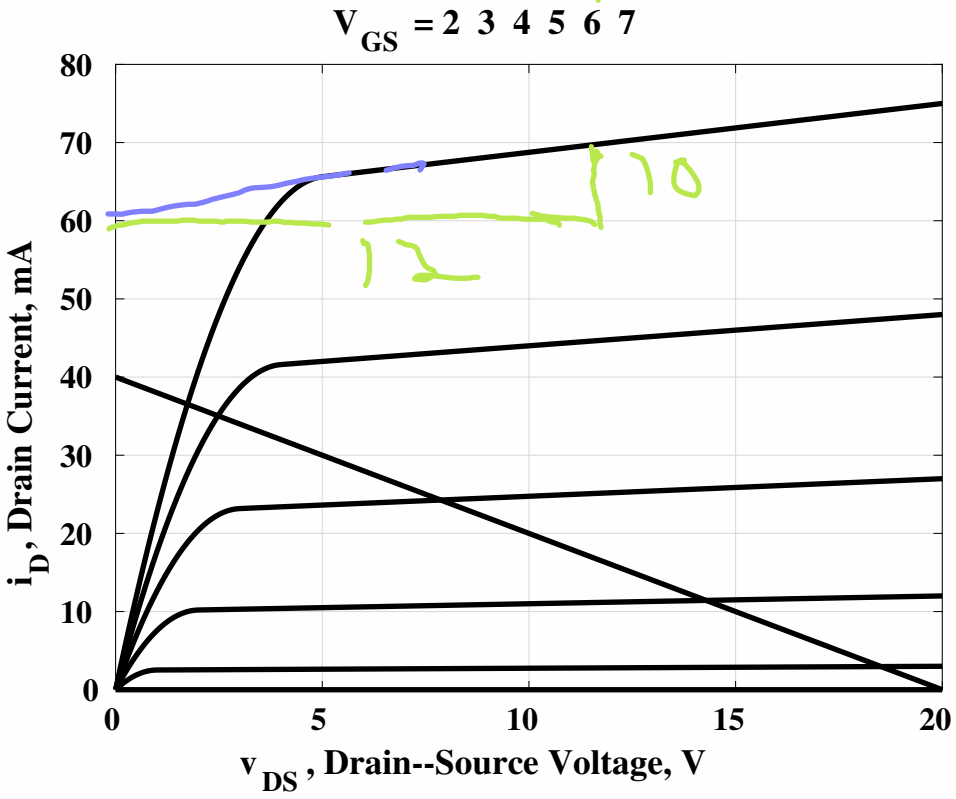
2 Reading the FET Curves

The figure shows a set of I–V curves for a particular NFET.
From the graph, determine the following (Assume $kp = 50\ \mu\text{A/V}^2$);

Threshold Voltage, $V_{t0} =$ 2 Volts

Width/Length Ratio, $W/L =$ 96 (actual 100)

Approximate Early Voltage, $V_A =$ 72 (actual 100) Volts



$K =$

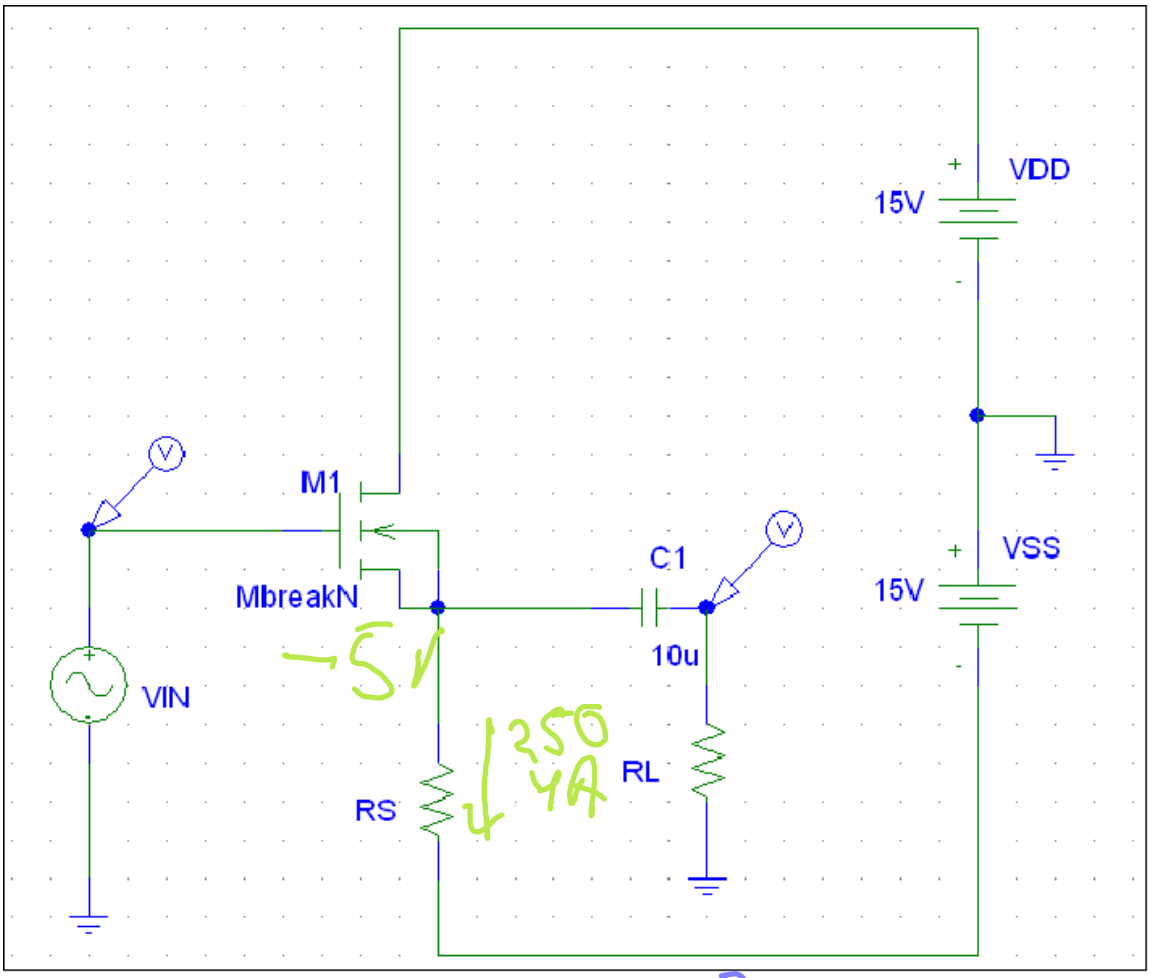
$$\frac{60\text{ mA}}{(7-2\text{V})^2} = 2.4\ \text{mA/V}^2$$

$$K = \frac{KP}{2}\frac{W}{L} \qquad \frac{W}{L} = \frac{2K}{KP} = 96$$

$$\frac{60\text{ mA}}{V_A} = \frac{10\text{ mA}}{12\text{ V}} \qquad V_A = 72\text{ V}$$

3 Discrete FET Amplifier

The following figure shows an amplifier using a discrete FET and a resistor. The transistor has a drain current of 250 μAmp when $V_{GS} = 5$ Volts, and the threshold voltage is zero. The Early Voltage is $V_A = 70$ Volts.



What type of amplifier is it? Common Drain

What is the typical situation in which this amplifier is used?

When a Voltage gain ≈1 is needed to drive a low impedance load.

3.1 Circuit Design

We want a drain current of 250 μAmperes in this circuit. What resistance do we need for RS?

$\frac{5v - (+5v)}{250\,uA} = 40k$

$R_S =$ 40k

3.2 Small–Signal Parameters

What are the small–signal parameters?

$g_m = \frac{2 \cdot 250\,uA}{V_{GS} - V_{TO}} = \frac{500\,uA}{5v}$

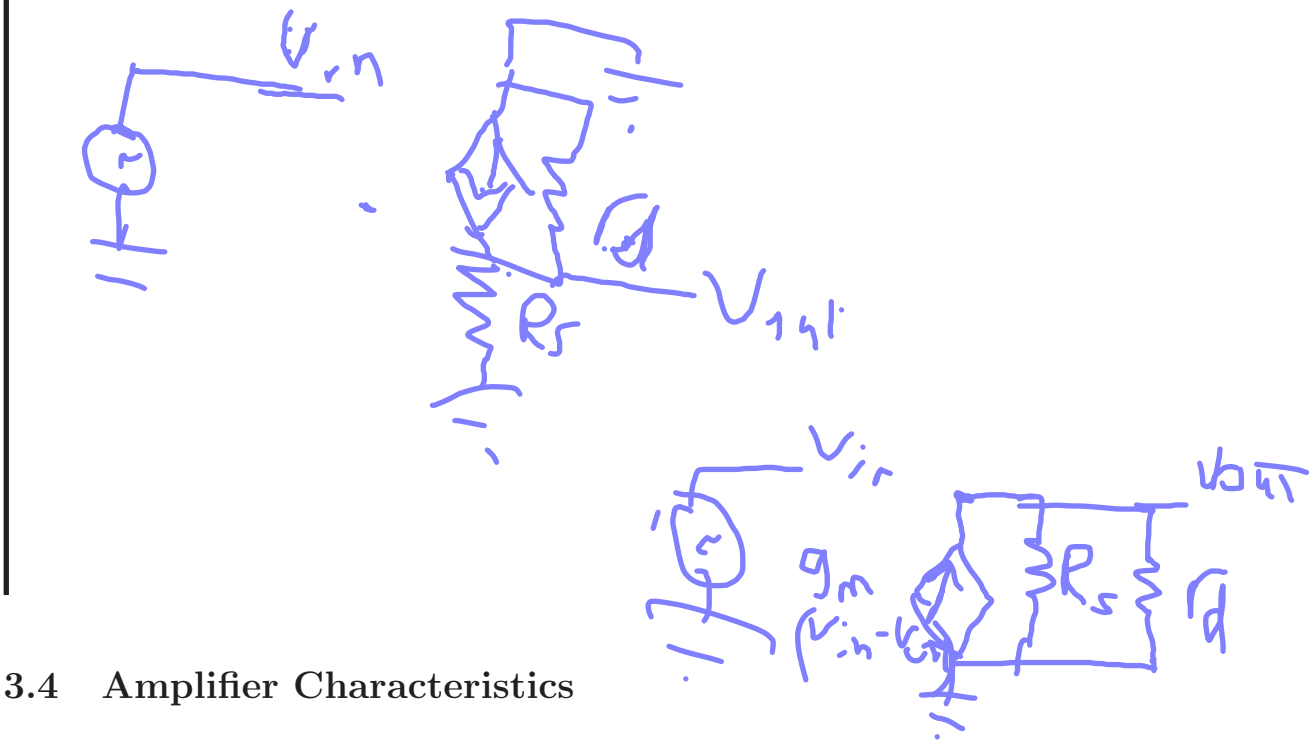
$r_d = \frac{70v}{250\,uA} = 280k$

$g_m =$ 100 uA/V

$R_0 =$ 280k (I meant r_d)

3.3 AC Circuit

Draw the AC circuit, using a Pi model for the transistor.



3.4 Amplifier Characteristics

What are the AC characteristics of this amplifier?

$$V_{out} = g_m (V_{in} - V_{out}) R_s \| r_d$$

$$V_{out}(1 + g_m R_s \| r_d) = V_{in} g_m R_s \| r_d$$

$$A_V = \frac{g_m R_s \| r_d}{1 + g_m R_s \| r_d} = \frac{5.5}{1 + 3.5}$$

Open–Circuit Gain 0.78

Input Resistance ∞

Output Resistance 35 k $\quad 40k \| 280k$

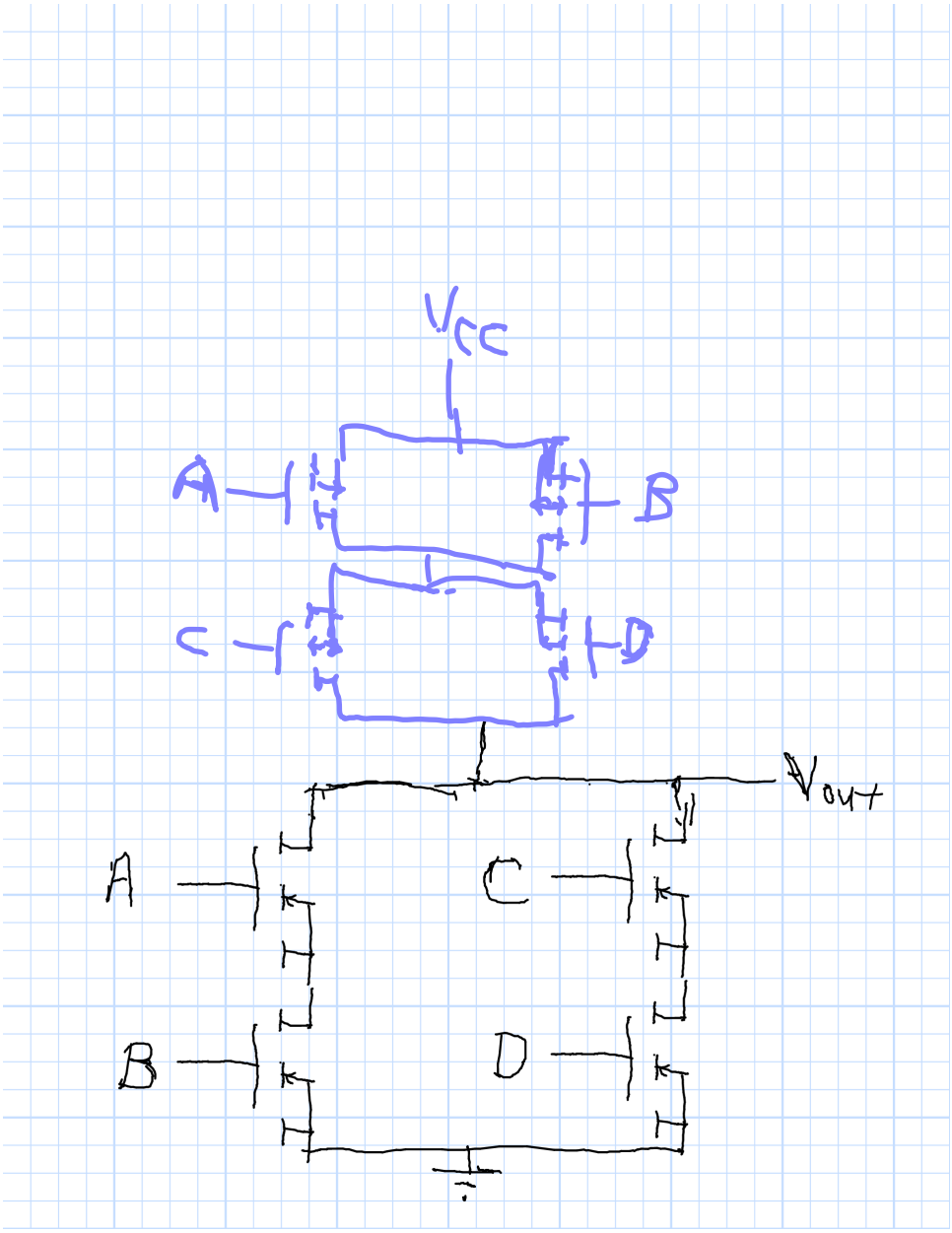
4 CMOS Logic

Consider the pull–down network in the figure.

4.1 Finish the Circuit

On the figure, draw the correct pull–up network. Use a 5–volt power supply and assume 5 volt input/output represents true and zero represents false.

Write the logic function implemented by this circuit.



4.2 Truth Table

Generate the truth table for this circuit;

A	B	C	D	Output

4.3 Transition

Assume that B is TRUE and all other inputs are FALSE. Sketch approximately the output voltage and current through the transistors as functions of time if A goes from FALSE to TRUE in 1 ns. You need not put numbers on the current axis; indeed, you can not with the information I've given.

(Output Voltage *vs.* Time:)

(Transistor Current *vs.* Time:)