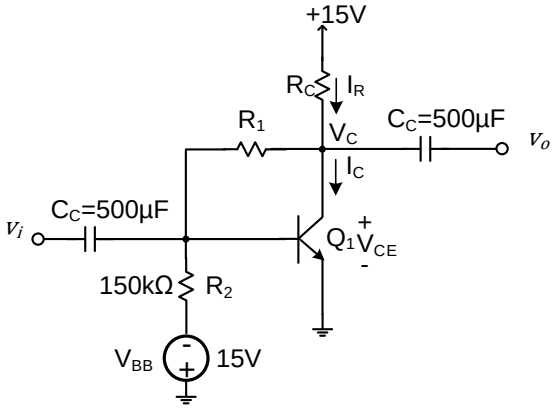
EECE 2412 – Homework 6 – Fall 2018

Due: Wednesday, October 31, 2018

1) Problem 4.35 on page 282 in the textbook.

2) Consider the circuit below, and assume that $V_{BE} = 0.7V$ and $\beta = 150$.
   a) DC analysis: Find the values of R_1 and R_C such that the bias point is with $V_{CE} = 6V$ and $I_C = 1.5mA$.
   b) Setup the circuit with your calculated values in PSpice, and simulate it to verify your results. Use the procedure described in homework 5 to model the BJT with the Qbreakn device model and a specified value of β. To avoid error messages related to the floating terminals of the capacitors at the input and output, you can connect 10GΩ resistors from v_i and v_o to ground. Alternatively, you can simulate the circuit without the capacitors to obtain the DC operating point information. Submit the schematics that show the DC collector current value.
   c) Small-signal parameter calculation: Calculate the small-signal parameters g_m, r_π, and r_{ce} at room temperature (300K) based on the results from part a), assuming that the Early voltage (V_A) is 100V (refer to the slides from lecture 18 or 19).
   d) Draw the small-signal equivalent circuit using the hybrid-π model that includes the parameters from part c). FYI: This is the circuit that you could use for AC analysis at mid-band frequencies (gain, input/output impedance, etc.).
   e) Replace the Qbreakn BJT model with the Q2N2222 model. Simulate the circuit again and submit a schematic that shows the DC current of the new operating point. Sweep the DC bias voltage at the base (V_{BB}) from 10V to 20V using the Q2N2222 transistor model for the BJT. Plot V_C vs. V_{BB}, and label the V_{BB} value at which V_C is equal to 5V. Submit the labeled plot.



3) Problem 4.20 on page 281 of the textbook (Allan R. Hambley, Electronics, 2nd edition). Provide the values of V_{CE} and I_B for the minimum and maximum Q-points. Is the output voltage signal at the collector terminal clipped? Show detailed analysis steps as well as print outs of your PSPICE schematic and simulation results.
   a) Perform load-line analysis as requested in the problem statement.
   b) Use PSPICE to verify your results as instructed in the problem statement.
      i. Select the Qbreakn transistor in the schematic and choose "edit → PSPICE model" in the menu on the top. To specify a β value of 300 and the I_S value of 10^{-12}A, change the statement in the first line to:

         .model Qbreakn NPN BF=300 IS=1e-12

         Save the model entry before running DC bias point simulation.
      ii. Print out the schematic that shows the voltage and currents from the DC bias point simulation.

iii. Switch to the simulation output window (in which you usually plot results). Choose "View → output file" in the menu on the top. Scroll down to the BJT model parameters and verify that BF is 300 for the Qbreakn device. Scroll down further to find the operating point information, which will be saved when the option is selected as described in part a). Notice that you can find a lot of relevant information in this list, such as V_{BE}, g_m, f_t, RO (= r_{ce}), RPI (= r_π). You can use these DC operating point and small-signal parameters when you want to perform accurate hand calculations. There are two parameters for β in the list: BETADC represents the DC current gain, and BETAAC represents the AC current gain. What are these two parameters for the BJT under the simulated DC bias conditions? Print out the output file and highlight BF, BETAAC, and BETADC for the transistor.

iv. Also print out the transient waveforms of $v_{in}(t)$, $i_B(t)$, and $v_O(t)$ [voltage at the collector of the BJT] for the homework submission.