EECE 2412 – Homework 12 – Fall 2018

Due: Wednesday, December 5, 2018

1) Problem 6.10 on page 406 in the textbook.

2) Problem 6.22 on page 406 in the textbook.

3) Review the material that you read in Section 6.4 of the textbook, and then solve problem 6.26 on page 407 in the textbook.

4) Design a CMOS inverter with a DC transfer characteristic in which the output transitions between logic 0 and 1 ($V_o \approx 2.5V$) when the input is $V_{DD}/2 = 2.5V$. That is, the trip point should be located close to half of the 5V supply voltage.
   a) Find the required ratio (W_P/W_N) for the widths of the PMOS and NMOS transistors assuming the following parameters: $KP_N = \mu_n \cdot C_{ox} = 150\mu A/V^2$, $KP_P = \mu_p \cdot C_{ox} = 50\mu A/V^2$, $\lambda = 0.02V^{-1}$, $V_{toN} = 0.7V$, $V_{toP} = -1V$, $L = L_{min} = 0.6\mu m$.
   b) Select the transistor widths that make the maximum current during the transition equal to 3mA.
   c) Sketch the DC transfer characteristic of the inverter and label the trip point.

5) Problem 6.66 on page 410 in the textbook. Note that the problem statement is asking for a 3-input NOR gate instead of a 2-input gate as in the mentioned example.

6) Sketch a suitable pull-up network (PUN) and the corresponding pull-down network (PDN) to realize a complex CMOS logic gate whose output has the following logic function: $Y = \bar{A} \cdot \overline{(B + C)}$.

7) Write the logic function [in the form Y = f(A,B,C,D)] that is realized by the complex logic gate below.