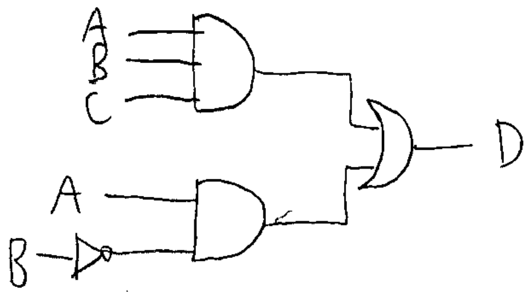
P.1

EECE 2412 – HW 10 Solutions

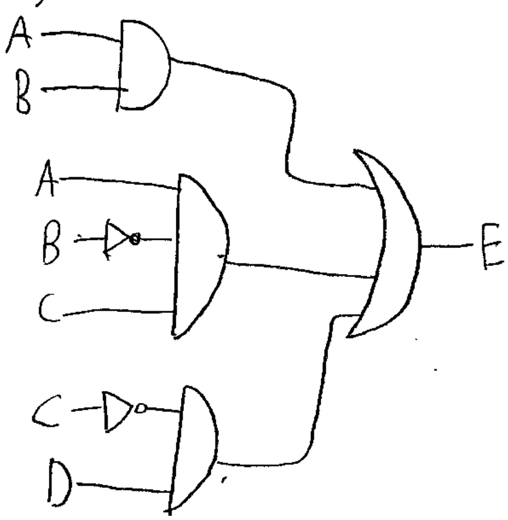
Problem 1

a) $D = ABC + A\bar{B}$



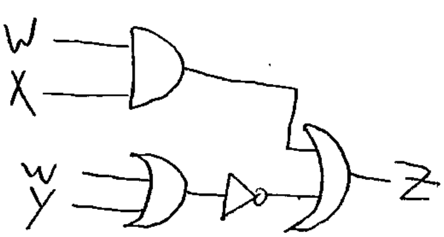
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

b) $E = AB + A\bar{B}C + \bar{C}D$



A	B	C	D	E
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

c) $Z = WX + \overline{(W+Y)}$



W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Hint: Find which inputs result in "1", then fill the rest with "0"

Problem 2

$NM_H = V_{OH} - V_{IH} = 4.5V - 3V = \boxed{1.5V = NM_H}$

$NM_L = V_{IL} - V_{OL} = 1.5V - 1V = \boxed{0.5V = NM_L}$

Problem 3

a) $$t_{PHL} = \frac{C_L \cdot V_{DD}}{\left(\frac{W}{L}\right)_N \cdot KP_N \cdot (V_{DD} - V_{toN})^2} = \frac{2\times10^{-12} \cdot 5}{\left(\frac{3}{1}\right) \cdot 50\times10^{-6}(5-1)^2}$$

$t_{PHL} = 4.167\times10^{-9}s = \boxed{4.167\ ns = t_{PHL}}$

$$t_{PLH} = \frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_P \cdot KP_P \cdot (V_{DD} - |V_{toP}|)^2} = \frac{2\times10^{-12} \cdot 5}{\left(\frac{6}{1}\right) \cdot 25\times10^{-6}(5-1)^2}$$

$\boxed{t_{PLH} = 4.167ns}$

b) same equations, but with $\left(\frac{W}{L}\right)_N = 3$ (no change)

$\left(\frac{W}{L}\right)_P = 60$ (new)

$t_{PHL} = 4.167ns$

$t_{PLH} = 0.4167ns$

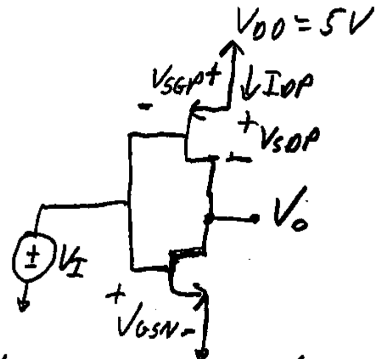
c) same equations with $\left(\frac{W}{L}\right)_N = 30$

$\left(\frac{W}{L}\right)_P = 6$

$t_{PHL} = 0.4167ns$

$t_{PLH} = 4.167ns$

Problem 4



a) Conditions at the trip point:

$V_I = \frac{V_{DD}}{2} = 2.5V$

$V_{GSN} = V_I - 0 = 2.5V$

It is required that $V_o = \frac{V_{DD}}{2} = 2.5V$, which implies that $I_{DP} = I_{DN}$

$V_{DSN} = V_o - 0V = 2.5V > V_{GSN} - V_{toN} = 2.5V - 0.7V = 1.8V$

$V_{DSN} > V_{GSN} - V_{toN}$ & $V_{GSN} > V_{toN}$ → The NMOS is in saturation at the trip point

$V_{SGP} = 5V - V_I = 2.5V > |V_{toP}| = 1V$

$V_{SGP} - |V_{toP}| = 2.5V - |-1V| = 1.5V$

$V_{DSP} = 5V - V_o = 2.5V > V_{SGP} - |V_{toP}|$ → the PMOS is in saturation

Equating the currents at the trip point, using the equations for the saturation region:

$I_{DP} = I_{DN}$

$$\left(\frac{W_P}{L_{min}}\right) \cdot \left(\frac{KP_P}{2}\right) \cdot \left(V_{SGP} - |V_{toP}|\right)^2 \cdot \left(1 + \lambda \cdot V_{SDP}\right)$$

$$= \left(\frac{W_N}{L_{min}}\right)\left(\frac{KP_N}{2}\right) \cdot \left(V_{GSN} - V_{toN}\right)^2 \cdot \left(1 + \lambda \cdot V_{DSN}\right)$$

↳ $W_P \cdot (50 \times 10^{-6}) \cdot (2.5 - 1)^2 \cdot (1 + 0.02 \cdot 2.5)$

$= W_N \cdot (150 \times 10^{-6}) \cdot (2.5 - 0.7)^2 \cdot (1 + 0.02 \cdot 2.5)$

↳ $\boxed{\frac{W_P}{W_n} = 4.32}$

... Prob. 14 cont.:

b) The peak current occurs at the trip point (Fig. 6-33 in the textbook)

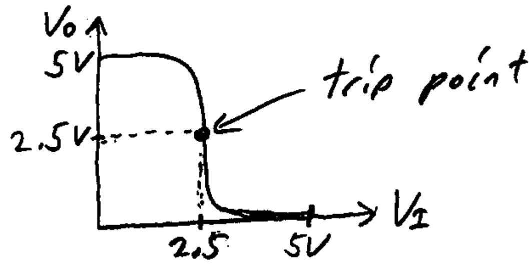
$$I_{DN} = 3\times10^{-3} = \left(\frac{W_N}{L_{min}}\right)\cdot\left(\frac{KP_N}{2}\right)\cdot\left(V_{GSN}-V_{THN}\right)^2\cdot\left(1+\lambda\cdot V_{DSN}\right)$$

$$3\times10^{-3} = \left(\frac{W_n}{0.6\times10^{-6}}\right)\cdot\left(\frac{150\times10^{-6}}{2}\right)\cdot(2.5-0.7)^2\cdot(1+0.02\cdot2.5)$$

↳ $W_N = 6.8\,\mu m$

$$W_P = \left(\frac{W_P}{W_N}\right)\cdot W_N = 4.32\cdot6.8\times10^{-6} = 29.4\,\mu m = W_P$$

c)



Problem 5

Using equation 6.7 in the textbook:

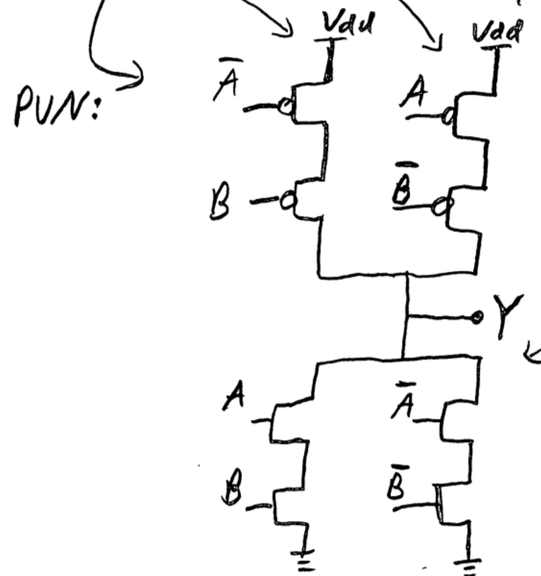
$$P_{dynamic} = f\cdot C_L\cdot(V_{DD})^2 = (100\times10^6\,Hz)\cdot(100\times10^{-15}F)\cdot(3V)^2$$

$P_{dynamic} = 90\,\mu W$

Problem 6

$$Y = A\bar{B} + \bar{A}B \rightarrow \bar{Y} = \overline{A\bar{B} + \bar{A}B} = \overline{A\bar{B}} \cdot \overline{\bar{A}B}$$

$$\bar{Y} = (\bar{A}+B)\cdot(A+\bar{B}) = AB + \bar{A}\bar{B}$$



PDN

(other solutions are possible)

Problem 7

basic inverter:

$\frac{W_P}{L_P} = p \longrightarrow r_{dsip}$

$\frac{W_N}{L_N} = n \longrightarrow r_{dsiN}$

resistances when "turned on":

$t_{PHL}, t_{PLH} \propto r_{ds}$

$r_{ds} \propto \frac{1}{\left(\frac{W}{L}\right)}$

$\Rightarrow t_{PHL}, t_{PLH} \propto \frac{1}{\left(\frac{W}{L}\right)}$

The series resistances of the transistors in the gate should sum up to an equivalent resistance $\leq r_{dsip}$ (or $\leq r_{dsiN}$) for all input combinations, where the series resistances of the transistors between the output Y and Vdd (or ground) are added when the transistors are "turned on".

$\Downarrow$ $\frac{W}{L}$ ratios of the transistors in the gate

$$\boxed{M_1: \frac{W}{L} = p}$$

$$\boxed{M_2, M_3: \frac{W}{L} = 2 \cdot p}$$

↳ When "on": two transistors in series, each having a resistances of $r_{ds2,3} = \frac{r_{dsip}}{2}$

$$\boxed{M_4, M_5, M_6: \frac{W}{L} = 2 \cdot n}$$

↳ worst case M_4 and (M_5 or M_6) are "on": each transistors has a resistance of $\frac{r_{diN}}{2}$, such that the sum is equal to r_{dsiN}

↳ equivalent resistance if all transistors are "on":

$$r_{eq} = \underset{(M_4)}{\frac{r_{dsiN}}{2}} + \underset{(M_5 \,//\, M_6)}{\left(\frac{r_{dsiN}}{2} \,//\, \frac{r_{dsiN}}{2}\right)} = \frac{3 \cdot r_{dsiN}}{4} < r_{dsiN}$$