Electronics
EECE2412 — Fall 2009
Final Exam with Solutions

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1 BJT Amplifier

A BJT circuit is shown in Figure 1.1. The capacitor is large enough to be considered a short circuit in the AC model.

1.1 Transistor Pi Model

What is the value of the resistor in the Pi model, r_π? Write the equation and evaluate.

$$r_\pi = \beta \frac{V_T}{I_C^{(DC)}} = (\beta + 1)\frac{V_T}{I_E^{(DC)}}$$

$$r_\pi = (160 + 1)\frac{25 \times 10^{-3} V}{1 \times 10^{-3} A}$$

ANSWER: 4025Ω.

r_π	4025Ω.

1.2 Early Effect

Compute r_0, the resistor associated with the Early Effect.

$$r_0 = \frac{V_A}{I_C^{(DC)}} \approx \frac{V_A}{I_e^{(DC)}} = \frac{V_A}{I_C^{(DC)}} = 125 \text{ k}\Omega \tag{1.1}$$

r_0	125 kΩ

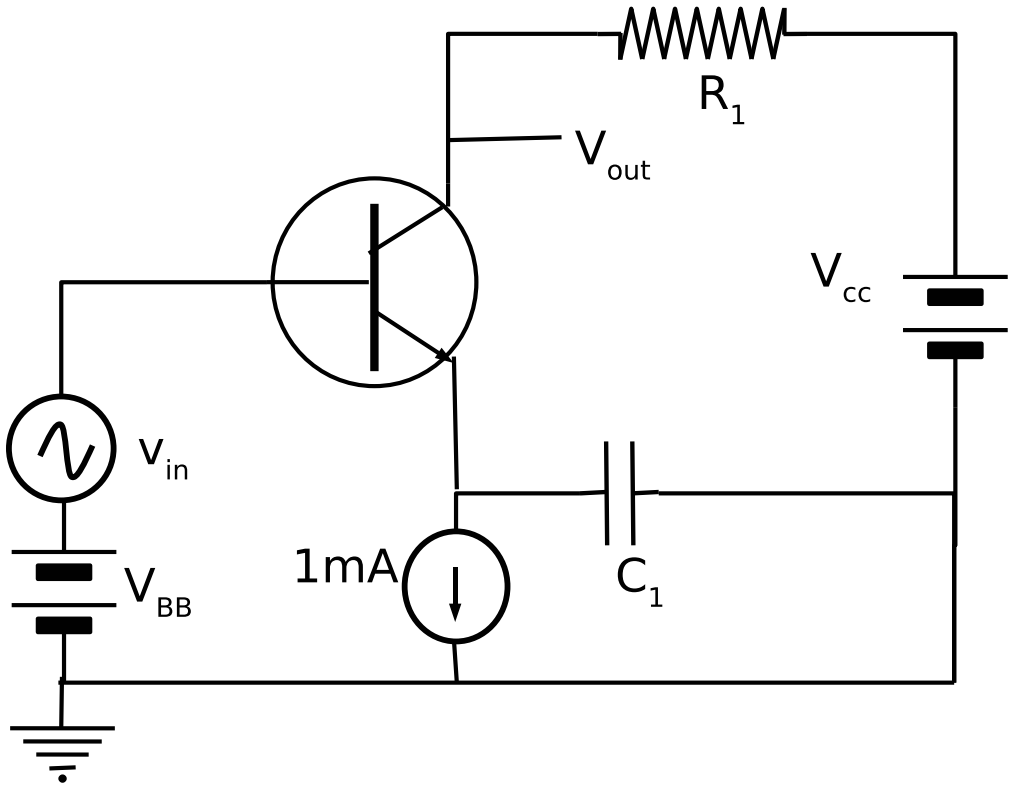

Figure 1.1: BJT circuit for Amplifier in Problem 1. The DC current is set at $I_E^{(DC)} = 1mA$, the transistor has a gain of $\beta = 160$, and $R_1 = 4k\Omega$. The Early Voltage is 125V.

1.3 Transconductance

Compute g_m, the transconductance.

$$g_m = \frac{I_C^{(DC)}}{V_T} = \frac{1mA}{25mV} = 0.04A/V \tag{1.2}$$

g_m	0.04 A/V

1.4 AC Circuit

Draw the AC circuit using a Pi model for the transistor.

See Figure 1.2.

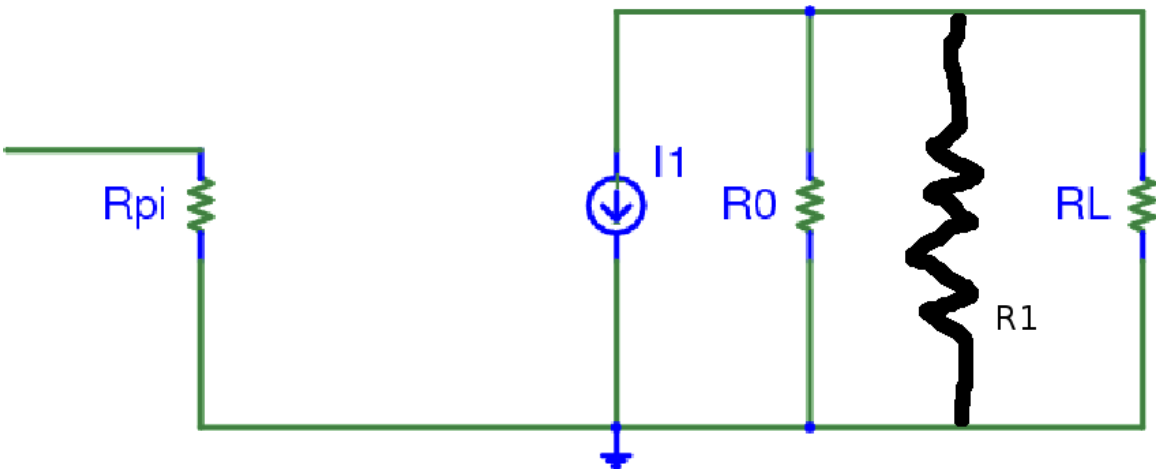

Figure 1.2: BJT Pi Model for Problem 1.

1.5 Voltage Gain

Write an equation for the voltage gain of the amplifier.

$$A_V = -g_m \left(r_0 \parallel R_1 \parallel R_L \right). \tag{1.3}$$

1.6 Application

What is the open–circuit gain? What is the gain with a load matched to the output resistance?

$$A_{Voc} = -g_m \left(r_0 \parallel R_1 \right) = -155. \tag{1.4}$$

With a matched load, it is half that, or

$$A_V = -g_m \left(r_0 \parallel R_1 \parallel R_1 \right) \approx -78. \tag{1.5}$$

A_{Voc}	-155
$A_{vMatched}$	-78

2 FET Amplifier

Consider the circuit in Figure 2.1. Here the transistor has the characteristics shown in Figure 2.2.

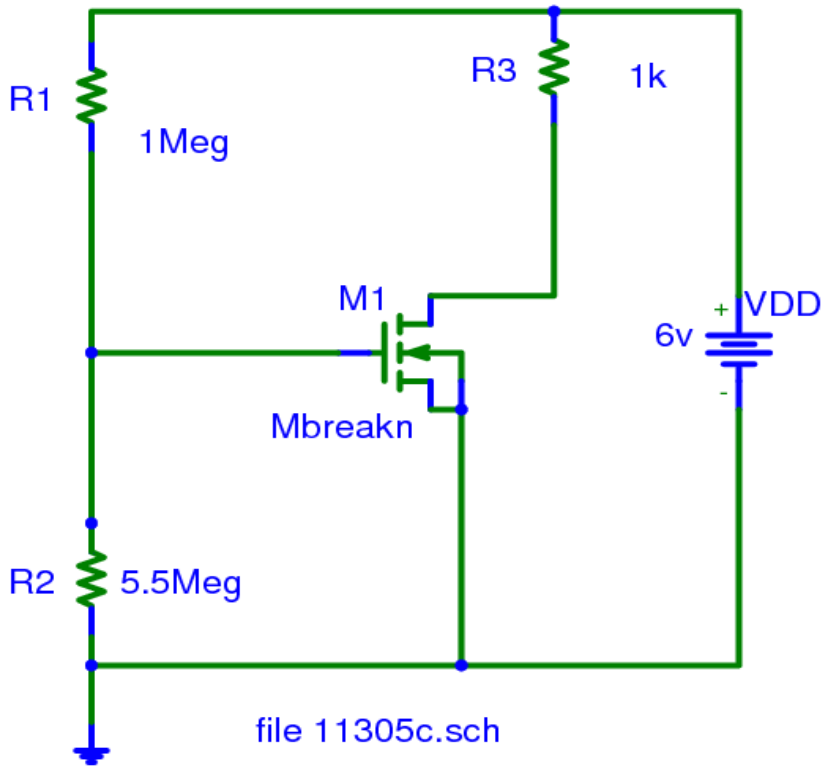

Figure 2.1: N–MOSFET Amplifier.

2.1 Bias

Find the bias point graphically, so that $I_D^{(DC)} = 4$ mA. What is the Drain–Source voltage?

$$V_{GS} = 5V \tag{2.1}$$

From the voltage divider.

Therefore,

from the curves,

$$V_{DS}^{(DC)} = 2 \text{ V}. \tag{2.2}$$

$V_{DS}^{(DC)}$	2 V

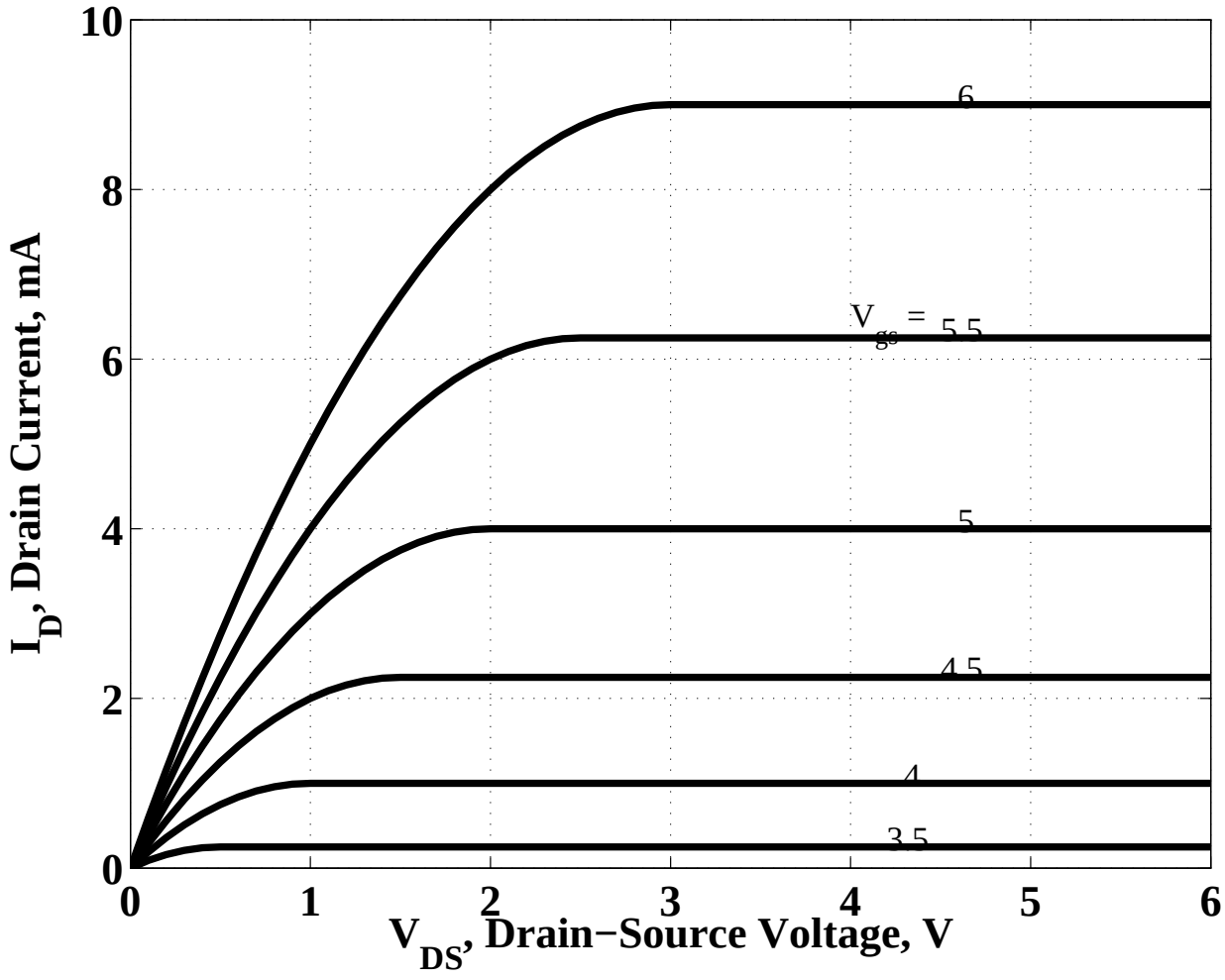

Figure 2.2: Curves for Transistors in the FET Amplifier. The output is at the connection between the drain and R3.

2.2 Transconductance

Compute the transconductance.

$$g_m = \frac{2I_D^{(DC)}}{V_{GS}^{(DC)} - V_{Thr}} \tag{2.3}$$

We need V_{thr}, which, from the curves must be 3 Volts.

$$g_m = \frac{2 \times 4 \text{ mA}}{5V - 3V} = 4 \times 10^{-3} A/V \tag{2.4}$$

g_m	$4 \times 10^{-3} A/V$

2.3 AC Circuit

Draw the AC circuit, using a Pi model for the transistor.

Usual with just the resistor R3.

2.4 Open–Circuit Voltage Gain

Compute the open–circuit voltage gain.

$$A_{Voc} = -g_m R_3 = 4 \times 10^{-3} A/V \times 10^3\ \Omega = -4 \tag{2.5}$$

A_{Voc}	-4

3 2–Stage Amplifier

Consider the circuit in Figure 3.1.

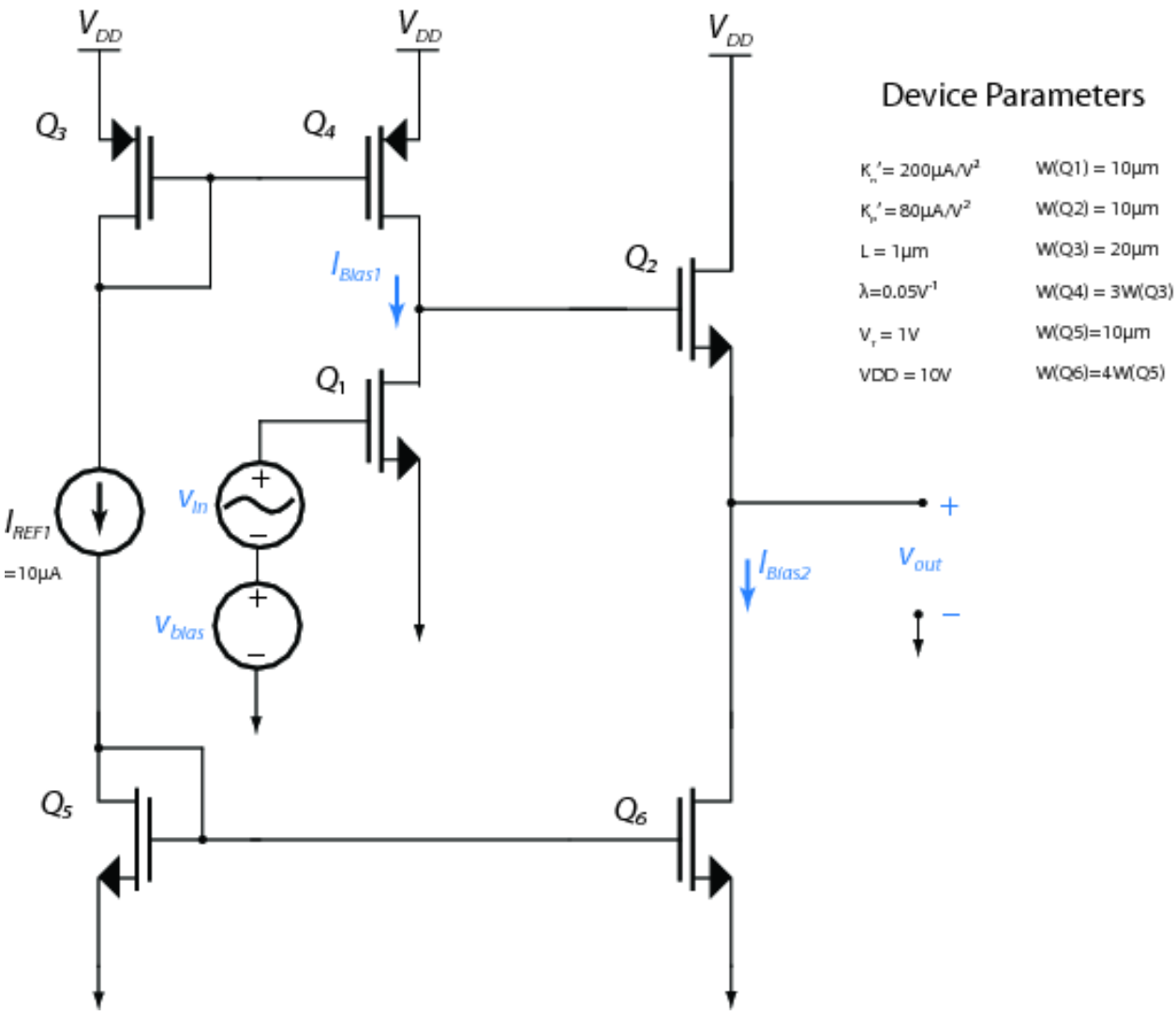

Figure 3.1: Two–Stage FET Amplifier. The device parameters (also shown in the upper right of the figure), are $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$ for the n–channel devices, $\mu_p C_{ox} = 80\ \mu\text{A/V}^2$ for the p–channel devices, $L = 1\ \mu$m for all, $\lambda = 0.05\ \text{V}^{-1}$ for all, $V_{thr} = 1$ V for all, $W(Q1) = 10\ \mu$m, $W(Q2) = 10\ \mu$m, $W(Q3) = 20\ \mu$m, $W(Q4) = 3W(Q3)$, $W(Q5) = 10\ \mu$m, $W(Q6) = 4W(Q5)$, and $V_{DD} = 10$ V.

3.1 Bias Currents

For parts 3.1 and 3.2, neglect channel length modulation ($\lambda = 0$ or $V_A \to \infty$)

Find the bias currents Ibias1 and Ibias2 and verify that Q1 and Q2 are in saturation.

$$I_{bias1} = 3I_{ref} = 30\ \mu\text{A} \tag{3.1}$$

$$I_{bias2} = 4I_{ref} = 40\ \mu\text{A} \tag{3.2}$$

Ibias1	30 μA
Ibias2	40 μA

3.2 Bias Voltage

For parts 3.1 and 3.2, neglect channel length modulation ($\lambda = 0$ or $V_A \to \infty$)

Determine the bias voltage (VBias) on Q1.

$$I_d = \mu_n C_{ox} \frac{W}{L} \frac{(V_{gs} - V_{thr})^2}{2} \tag{3.3}$$

Solve for V_{gs}

$$V_{gs} = \sqrt{2 I_{bias1} \frac{L}{\mu_n C_{ox} W}} + V_t =$$

$$\sqrt{2 \times 30 \times 10^{-6}\ \text{A} \frac{1\ \mu\text{m}}{10\ \mu\text{m} \times 200 \times 10^{-6}\ \text{A/V}^2}} + 1\ \text{V} \tag{3.4}$$

Vbias	1.17 V

3.3 Small–Signal Parameters

Find g_{m1}, g_{m2}, r_{o1}, r_{o2} and draw the small signal model for the two-stage amplifier. Don't forget the "Early" resistances of the current source transistors!

We use two different expressions for the transconductance, because it is hard to find V_{GS} for the second amplifier. For the first one,

$$g_{m1} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{thr}) \tag{3.5}$$

and for the second

$$g_{m2} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}. \tag{3.6}$$

$$r_0 = \frac{1}{\lambda I_D} \tag{3.7}$$

g_{m1}	346 μA/V
g_{m2}	400 μA/V
r_{o1}	667 kΩ
r_{o2}	500 kΩ

The small–signal circuit is shown in Figure 3.2. The two additional resistors (associated with the current sources, Q4 and Q6) are calculated from

$$r_0 = \frac{1}{\lambda I_D} \tag{3.8}$$

and are thus the same as those of the corresponding amplifier transistors.

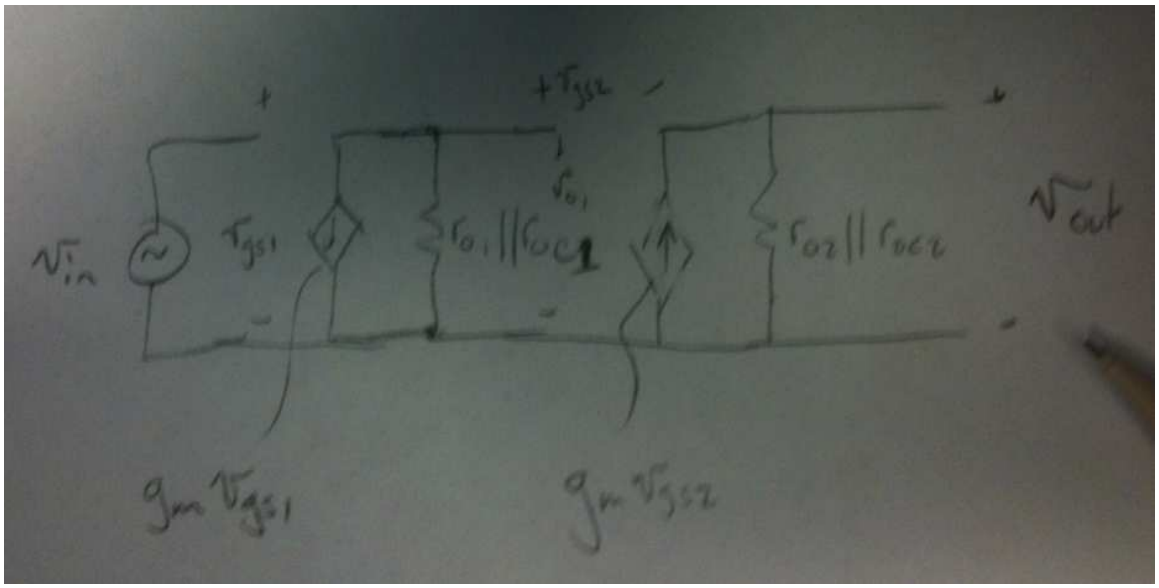

Figure 3.2: Small–Signal Model for Two–Stage Amplifier

3.4 Performance

Find A_{Voc1}, A_{Voc2}, and the total voltage gain of the amplifier.

$$A_{voc1} = -g_{m1}\left(r_{01} \parallel r_{01}\right) = -g_{m1}\frac{r_{01}}{2} \tag{3.9}$$

$$V_{in2} = V_{GS2} + V_{out} \tag{3.10}$$

$$V_{out} = g_{m2}V_{GS2}\left(r_{02} \parallel r_{02}\right) \tag{3.11}$$

$$A_{Voc2} = \frac{g_m}{g_m + \frac{2}{r_{02}}} \tag{3.12}$$

A_{Voc1}	-1.3×10^6
A_{Voc2}	≈ 1

3.5 Analysis

What do you notice about the gain of the second stage (The common-drain stage)? Why is it beneficial in this circumstance?

The output stage is a common–drain amplifier. As we discussed in class, the gain is near unity, and the purpose of using it is the low output impedance. Specifically

$$R_{out} = \frac{1}{g_{m2} + \frac{2}{r_{02}}} \approx g_{m2} \tag{3.13}$$

4 FET Logic

Consider the logic inverter shown in Figure 4.1, with the parameters shown in the caption.

4.1 Triode Equation

Write equations for i_D for the P–FET in triode operation, as a function of the supply voltage, V_1, the input voltage, V_2, and the output voltage, V_{out} at the location of the voltage marker in the figure.

$$i_D = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{SG} - V_{Thr}\right)V_{SD} - \frac{1}{2}V_{SD}^2\right] \tag{4.1}$$

$$i_D = \mu_n C_{ox}\frac{W}{L}\left[\left(V_1 - V_2\right)\left(V_1 - V_{out}\right) - \frac{1}{2}\left(V_1 - V_{out}\right)^2\right] \tag{4.2}$$

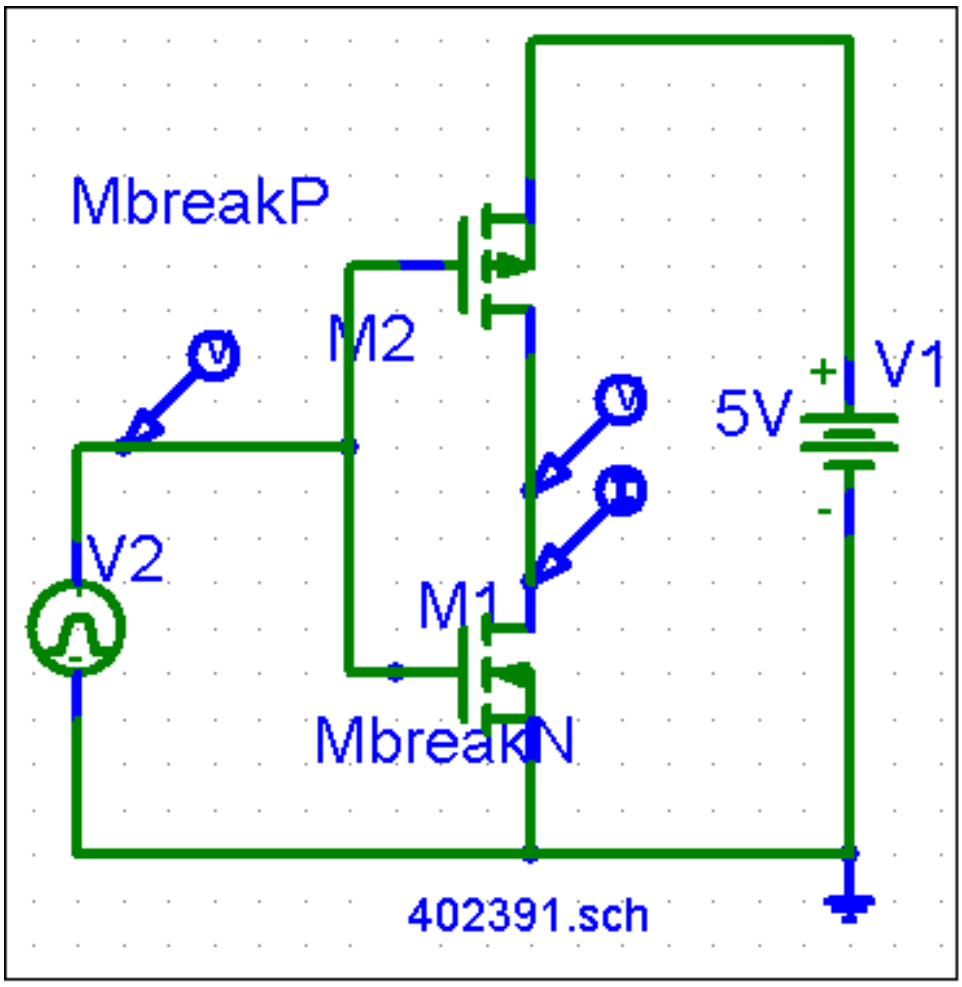

Figure 4.1: Circuit for the FET Inverter. Both transistors have thresholds of 0 Volts, and $\mu C_{ox} W/L = 40\ \mu\text{A/V}^2$.

4.2 Saturation Equation

Write equations for i_D for the N–FET in saturation, as a function of the supply voltage, V_1 the input voltage, V_2, and the output voltage, V_{out} at the location of the voltage marker in the figure. .

$$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{Thr})^2}{2} \tag{4.3}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \frac{V_2^2}{2} \tag{4.4}$$

4.3 Solution

Let the input voltage be either $V_2 = 4.8$ V or $V_2 = 0.2$ V. Solve the equations for the output voltage, V_{out}, and determine which of the two input voltages is appropriate for this situation.

Combine Equations 4.2 and 4.4.

$$(V_1 - V_2)(V_1 - V_{out}) - \frac{1}{2}(V_1 - V_{out})^2 = \frac{V_2^2}{2} \tag{4.5}$$

$$V_1^2 + V_2 V_{out} - V_1 V_{out} - V_1 V_2 - \frac{V_1^2}{2} + V_1 V_{out} - \frac{V_{out}^2}{2} - \frac{V_2^2}{2} = 0 \tag{4.6}$$

$$\frac{V_1^2}{2} + V_2 V_{out} - V_1 V_2 - \frac{V_{out}^2}{2} - \frac{V_2^2}{2} = 0 \tag{4.7}$$

$$V_{out}^2 - 2V_2 V_{out} - V_1^2 + 2V_1 V_2 + V_2^2 = 0 \tag{4.8}$$

In the quadratic equation, for $V_2 = 4.8$ V or $V_2 = 0.2$ V

$$a = 1 \tag{4.9}$$

$$b = -2V_2 (= -9.6,\ -0.4\ \text{V}) \tag{4.10}$$

$$c = -V_1^2 + 2V_1 V_2 + V_2^2 (= 46,\ -23\ \text{V}^2) \tag{4.11}$$

Then,

$$b^2 - 4ac = (-92,\ 92\ \text{V}^2) \tag{4.12}$$

The result must be positive. Therefore, the LOWER INPUT VOLTAGE is the correct one.

$$v_{out} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = 4.99\ \text{V} \tag{4.13}$$

4.4 Power Consumption

Compute the current and the power consumed by the inverter in this condition.

Use Equation 4.4 to find the current

$$i_D = \mu_n C_{ox} \frac{W}{L} \frac{V_2^2}{2} = 40 \times 10^{-6}\ \text{A/V}^2 \frac{0.262}{2} = 8 \times 10^{-7} A \tag{4.14}$$

The current passes through both transistors, so the total voltage drop is V_1, so

$$P = i_D \times V_1 = 4 \times 10^{-6} \text{ W} \tag{4.15}$$

Current	8×10^{-7} A
Power	4×10^{-6} W