

Electronics
EECE2412 — Fall 2009
Final Exam

Prof. Charles A. DiMarzio
Department of Electrical and Computer Engineering
Northeastern University

Doc:11419

16 December 2009

Name: _____

General Rules:

- You may make use of one sheet of notes, 8.5-by-11 inches, using both sides of the page, and one copy of the FET equations table from Hambley.
- You may use a calculator.
- Present your work as clearly as possible. I give partial credit if I can figure out that you know what you are doing. I do not give credit for putting down everything you know and hoping I will find something correct in it.
- Each question has a vertical black bar providing space for your work and a box for numerical answers. Please write your answer to each question clearly. If it happens to be correct, I give you points quickly and move on to the next problem. Please show your work in the space provided, or on extra pages, clearly labeled with the problem number. If the answer is wrong, this will make it easy for me to find ways to give you partial credit.
- Avoid any appearance of academic dishonesty. Do not talk to other students during the exam. Keep phones, computers, and other electronic devices other than calculators secured and out of reach.

1 BJT Amplifier

A BJT circuit is shown in Figure 1.1. The capacitor is large enough to be considered a short circuit in the AC model.

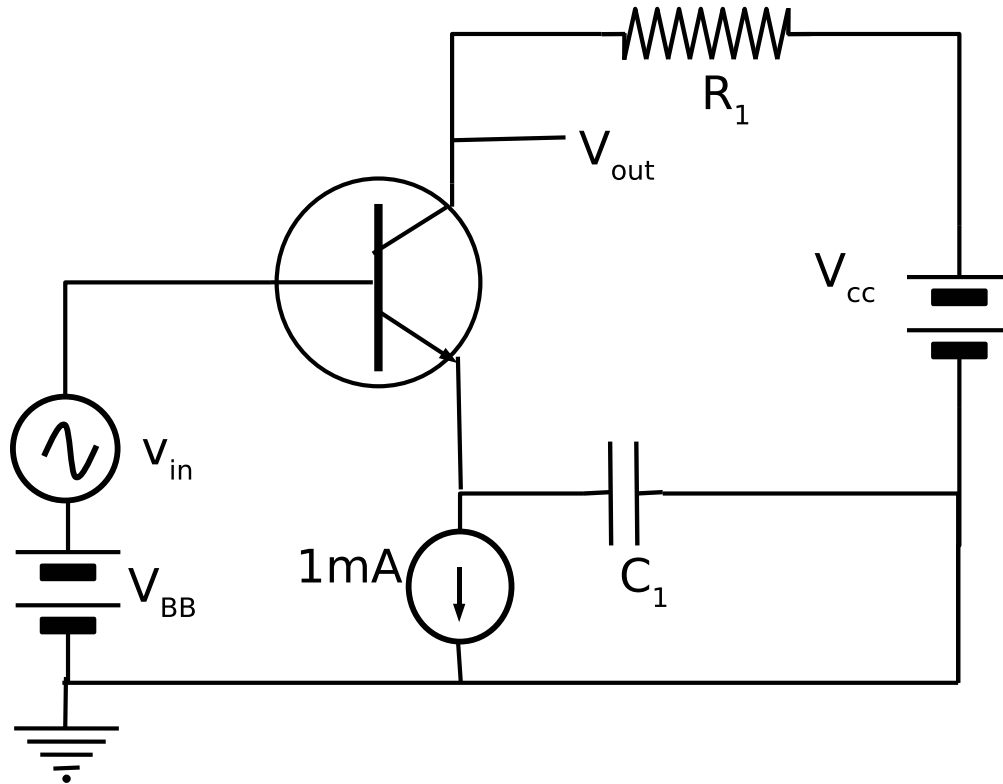


Figure 1.1: BJT circuit for Amplifier in Problem 1. The DC current is set at $I_E^{(DC)} = 1\text{mA}$, the transistor has a gain of $\beta = 160$, and $R_1 = 4\text{k}\Omega$. The Early Voltage is 125V .

1.1 Transistor Pi Model

What is the value of the resistor in the Pi model, r_π ? Write the equation and evaluate.

r_π	
---------	--

1.2 Early Effect

Compute r_0 , the resistor associated with the Early Effect.



r_0	
-------	--

1.3 Transconductance

Compute g_m , the transconductance.



g_m	
-------	--

1.4 AC Circuit

Draw the AC circuit using a Pi model for the transistor.



1.5 Voltage Gain

Write an equation for the voltage gain of the amplifier.

|

1.6 Application

What is the open-circuit gain? What is the gain with a load matched to the output resistance?

|

A_{Voc}	
$A_{vMatched}$	

2 FET Amplifier

Consider the circuit in Figure 2.1. Here the transistor has the characteristics shown in Figure 2.2.

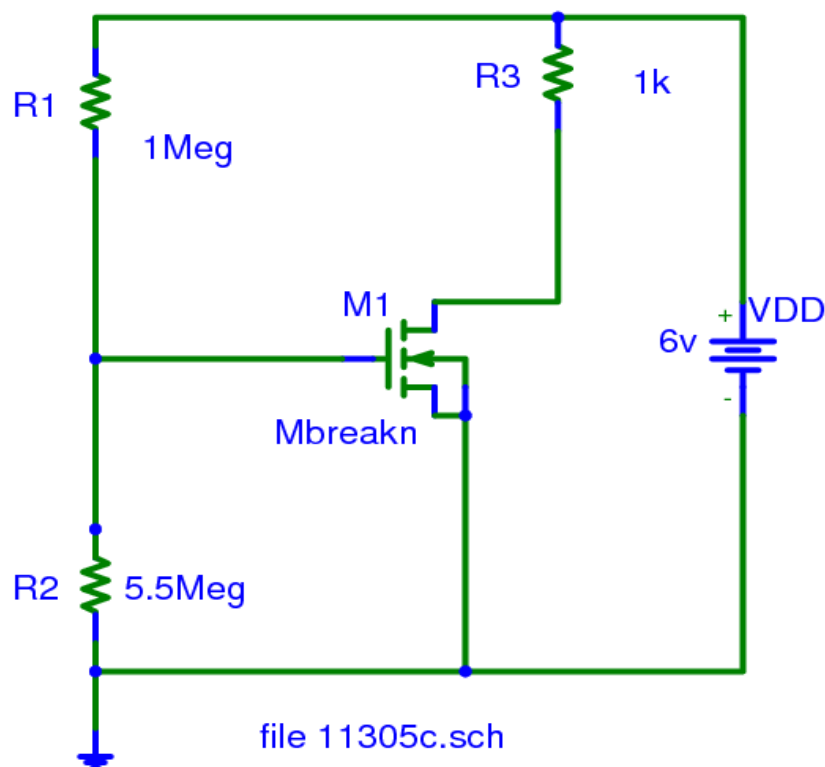


Figure 2.1: N-MOSFET Amplifier.

2.1 Bias

Find the bias point graphically, so that $I_D^{(DC)} = 4 \text{ mA}$. What is the Drain-Source voltage?

$V_{DS}^{(DC)}$	
-----------------	--

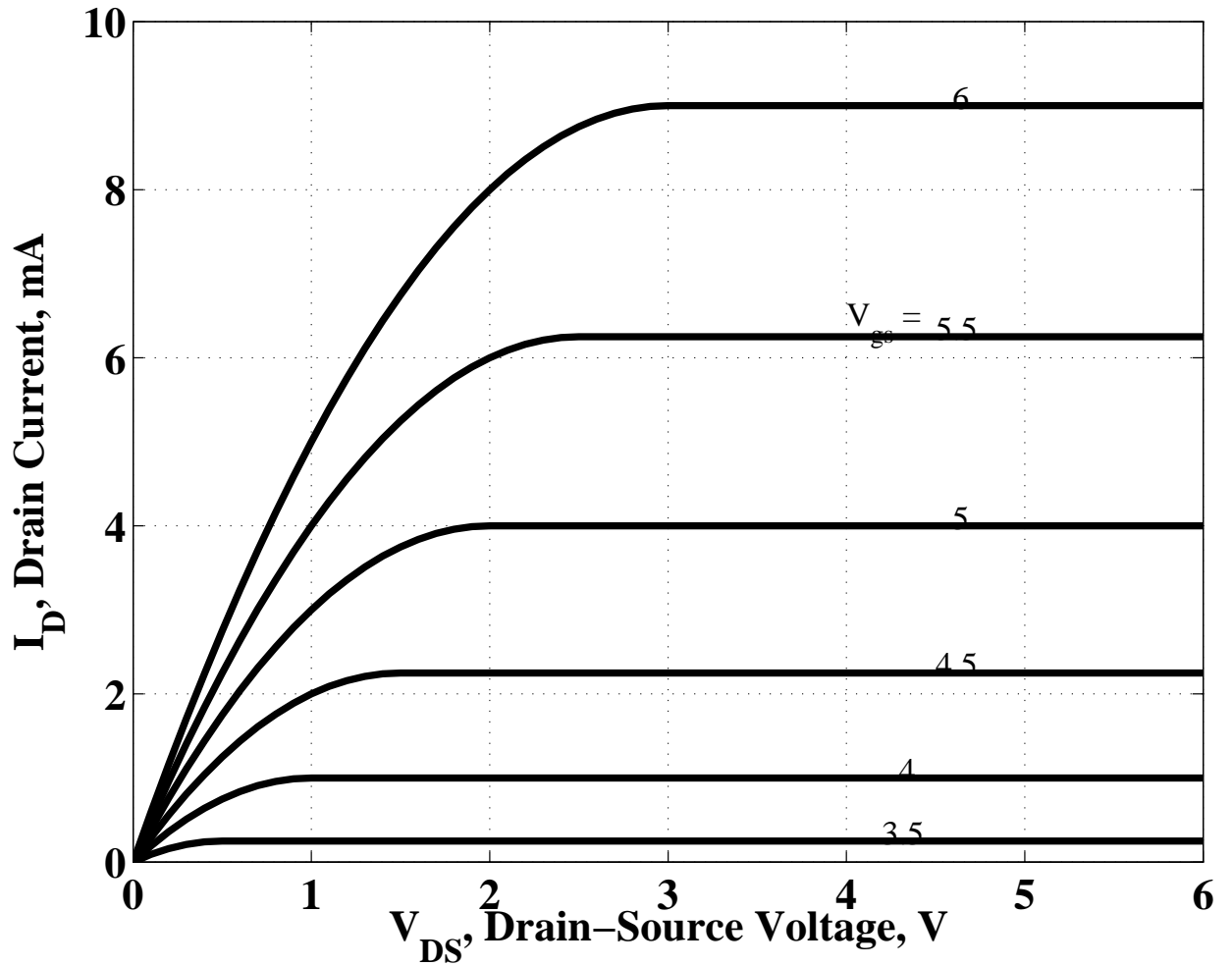


Figure 2.2: Curves for Transistors in the FET Amplifier. The output is at the connection between the drain and R3.

2.2 Transconductance

Compute the transconductance.

|

g_m	
-------	--

2.3 AC Circuit

Draw the AC circuit, using a Pi model for the transistor.



2.4 Open-Circuit Voltage Gain

Compute the open-circuit voltage gain.



A_{Voc}	
-----------	--

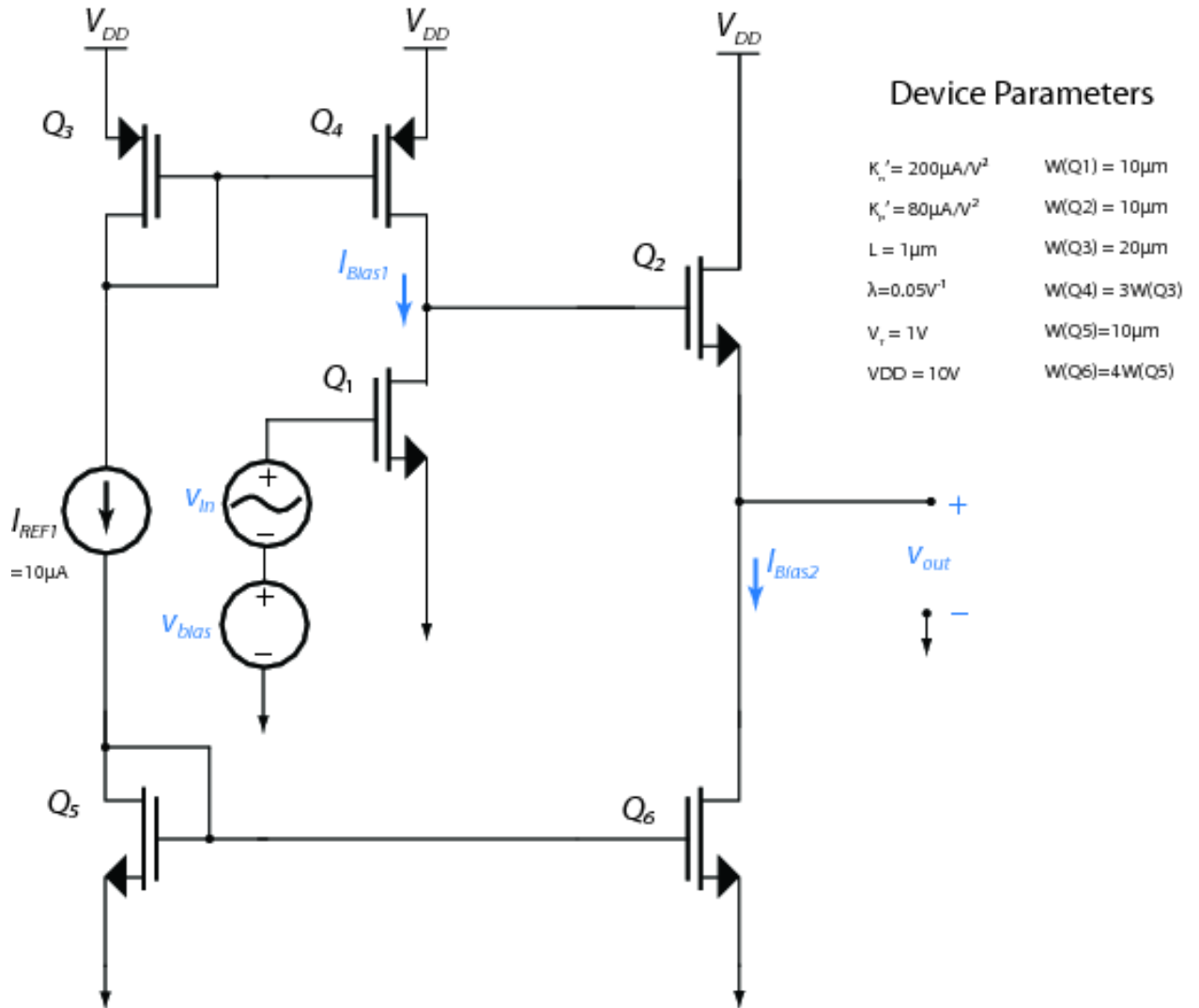


Figure 3.1: Two-Stage FET Amplifier. The device parameters (also shown in the upper right of the figure), are $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$ for the n-channel devices, $\mu_p C_{ox} = 80 \mu\text{A}/\text{V}^2$ for the p-channel devices, $L = 1 \mu\text{m}$ for all, $\lambda = 0.05 \text{V}^{-1}$ for all, $V_{thr} = 1 \text{V}$ for all, $W(Q1) = 10 \mu\text{m}$, $W(Q2) = 10 \mu\text{m}$, $W(Q3) = 20 \mu\text{m}$, $W(Q4) = 3W(Q3)$, $W(Q5) = 10 \mu\text{m}$, $W(Q6) = 4W(Q5)$, and $V_{DD} = 10 \text{V}$.

3 2-Stage Amplifier

Consider the circuit in Figure 3.1.

3.1 Bias Currents

For parts 3.1 and 3.2, neglect channel length modulation ($\lambda = 0$ or $V_A \rightarrow \infty$)

Find the bias currents I_{bias1} and I_{bias2} and verify that Q1 and Q2 are in saturation.

I_{bias1}	
I_{bias2}	

3.2 Bias Voltage

For parts 3.1 and 3.2, neglect channel length modulation ($\lambda = 0$ or $V_A \rightarrow \infty$)

Determine the bias voltage (V_{Bias}) on Q1.

V_{bias}	
------------	--

3.3 Small-Signal Parameters

Find g_{m1} , g_{m2} , r_{o1} , r_{o2} and draw the small signal model for the two-stage amplifier. Don't forget the "Early" resistances of the current source transistors!



g_{m1}	
g_{m2}	
r_{o1}	
r_{o2}	

3.4 Performance

Find $A_{V_{oc1}}$, $A_{V_{oc2}}$, and the total voltage gain of the amplifier.



$A_{V_{oc1}}$	
$A_{V_{oc2}}$	

3.5 Analysis

What do you notice about the gain of the second stage (The common-drain stage)? Why is it beneficial in this circumstance?



4 FET Logic

Consider the logic inverter shown in Figure 4.1, with the parameters shown in the caption.

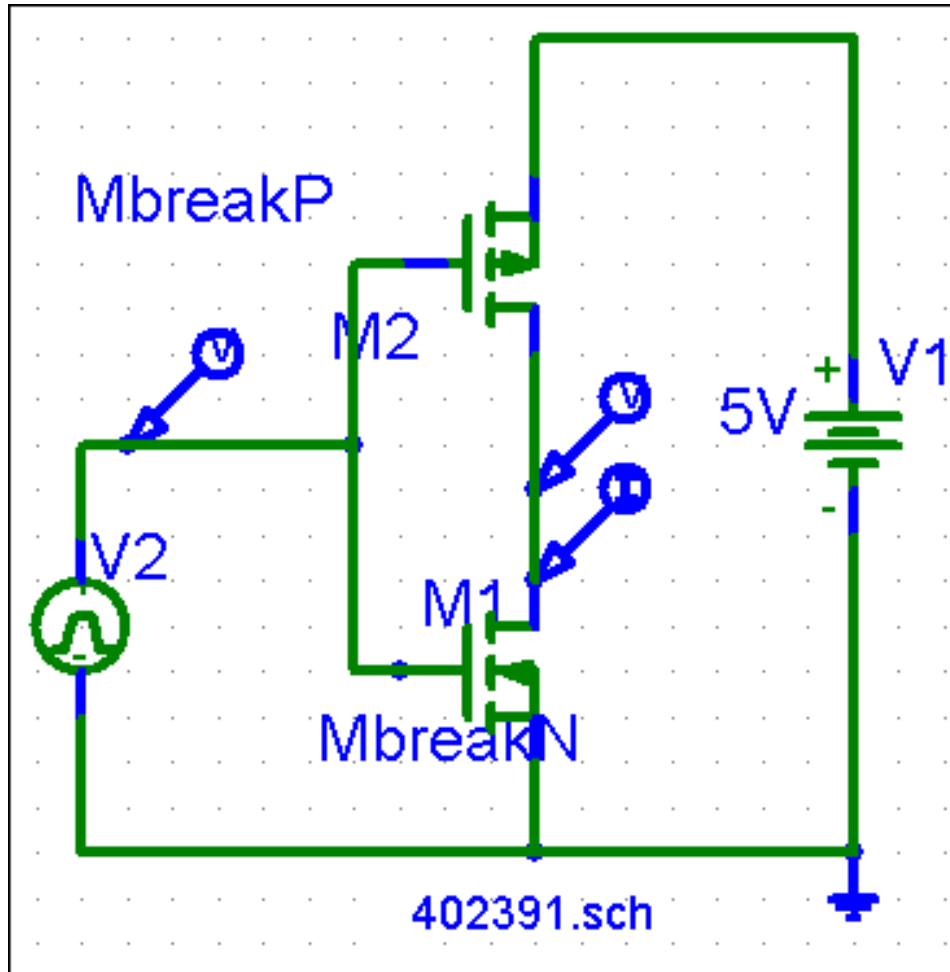


Figure 4.1: Circuit for the FET Inverter. Both transistors have thresholds of 0 Volts, and $\mu C_{ox} W/L = 40 \mu\text{A}/\text{V}^2$.

4.1 Triode Equation

Write equations for i_D for the P-FET in triode operation, as a function of the supply voltage, V_1 , the input voltage, V_2 , and the output voltage, V_{out} at the location of the voltage marker in the figure.



4.2 Saturation Equation

Write equations for i_D for the N-FET in saturation, as a function of the supply voltage, V_1 the input voltage, V_2 , and the output voltage, V_{out} at the location of the voltage marker in the figure. .



4.3 Solution

Let the input voltage be either $V_2 = 4.8 \text{ V}$ or $V_2 = 0.2 \text{ V}$. Solve the equations for the output voltage, V_{out} , and determine which of the two input voltages is appropriate for this situation.



4.4 Power Consumption

Compute the current and the power consumed by the inverter in this condition.



Current	
Power	