Chapter 4

The Properties and Applications of Operational Amplifiers

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The operational amplifier is an integrated circuit (IC) designed to provide voltage-controlled voltage sources. This very high-gain amplifier is the basic linear IC building block and many manufacturers fabricate as many as four identical units on a single chip. As a circuit element the operational amplifier or simply Op-amp is ubiquitous with applications in communication, control, instrumentation and data-conversion systems.

The name operational amplifier was coined by John R. Ragazzini[1] because of its ability to perform mathematical operations. Our objective in this chapter is to describe the Op-amp as a circuit element and introduce some of its basic applications. In addition, at the end of the chapter we introduce the analog multiplier. Used in conjunction with operational amplifiers, the range of application is significantly expanded.

[1]John R. Ragazzini, one of the author's mentors, was one of the pioneers of modern control systems both as a practitioner and teacher. During World War II he recognized that communication between a pilot and the airport tower constituted a control system. This was fundamental to the development of instrument landing systems. He was also one of the leading advocates for embedding computers within control systems.

4.1 Case Study: Analog Computation

How are the following characterized and determined?

1. The velocity of the Mars capsule carrying the rover Curiosity after its parachute deployed.
2. The blood alcohol level after a beer or two.
3. The impact of monetary, political and environmental factors on the change in value of financial instruments.
4. The speed and amplitude of a pulse as it is transmitted along a nerve from the source of the stimulus to the brain.
5. The response of the tuning circuit of a car's FM radio to a given station and one adjacent to it.
6. The vibration of an automobile after it hits a bump.
7. The diffusion of a metal into a semiconductor or another metal.
8. The pressure and volume of blood in an occluded coronary artery.
9. The variation in the temperature of a teaspoon's handle when its bowl is inserted into hot coffee.
10. The speed with which chemicals can combine in pharmaceutical processes.

The common denominator of the above is that they all are characterized by one or a system of differential equations. A question arises " Can we solve these equations electronically?" Clearly the answer is "yes", otherwise this exercise is irrelevant. Both analog and digital computers can solve differential equations with digital solutions overwhelmingly prevalent today. In the past Acey Deucy Electronics manufactured a desk top analog computer similar to the one displayed in Fig. 4.1. Acey Deucy's computer was capable solving eighth-order differential equations and sets of simultaneous equations containing eight unknowns. While such desk tops are now relics, the circuits and techniques employed are widely used in current systems. Let us now investigate how analog computers solved differential equations.

Analog computers are comprised of circuits called *integrators, amplifiers, summers,* and *function generators.* An integrator produces and output

$$-\frac{1}{K}\int_0^t f(\tau)d\tau$$

The amplifier's function is to scale its input by a constant, either positive or negative. The summer adds all of its inputs algebraically. The summer's output is expressible as

$$g(x) = a_1x_1 + a_2x_2 + \ldots + a_nx_n$$

where the a_i are constants and the x_i are the inputs. The laboratory instrument you use to obtain sine, square and triangular waveforms or a variety of frequencies and amplitudes is a function generator. The one in an analog computer is more complex as its output can approximate a large variety of mathematical waveforms.

Programming an analog computer requires connecting the various circuits to match the differential equation. Consider the second-order equation

$$\frac{d^2x}{dt^2} + a_1\frac{dx}{dt} + a_0x = f(t) \tag{1}$$

Recasting (1) results in

$$\frac{d^2x}{dt^2} = -a_1\frac{dx}{dt} - a_0x + f(t) \tag{2}$$

The program, i.e. the circuit connection, by which (2) is solved is shown in Fig. 4-2. As expected we must integrate d^2x/dt^2 twice to obtain $x(t)$. The output of Integrator I is scaled by Amplifier I to give $-a_1dx/dt$ which is both the input to Integrator II and one input to the Summer. Amplifier II scales the output of Integrator II to produce $x(t)$ which is both the result and the input to Amplifier III. The output of Amplifier III is $-a_0x$ the second Summer input. The function generator output is $f(x)$, the third Summer input whose output is d^2x/dt^2 in (2) and is the input to Integrator I.

Less hardware was used to solve for $x(t)$ than is used in a digital computer solution. Why is the digital computer universal and analog ones passe? A major reason is the answer to the following question: "What must we do to solve for $x(t)$ again with new values of a_1 and a_0?" In the analog domain we need to *change the hardware* whereas we *change the software* in the digital computer.

The circuits used in an analog computer are still used in practice. Present day IC technology allows for the fabrication of both analog and digital circuits on a single chip. Thus, operations better done using digital (analog) techniques are performed in the digital (analog) domain.

All the circuits used in the analog computer plus the digital-to-analog (DAC) and analog-to-digital (ADC) converters employ operational amplifiers the major subject of this chapter. The case study that opens the next section is the design of a practical operational amplifier and several of the issues that face the engineers responsible.

4.2 Operational Amplifier Characteristics

The circuit symbol of an Op-amp is shown in Fig. 4.3a. Two inputs v_1 and v_2 can be accommodated and v_o is the single output; each of these voltages is measured with respect to ground, the common reference node in the circuit. Figure 4.3b displays the equivalent circuit of the practical Op-amp as a four-terminal device. We observe that the strength of the dependent source is proportional to the difference voltage v_d as expressed in Eq. 4.1. Because of the

$$v_d = v_1 - v_2 \tag{4.1}$$

polarity of the controlled source, v_o is proportional to $-A_vv_d$. The minus and plus signs at the Op-amp input in Fig. 4.3a refer to the inverting and non-inverting terminals. That is, if $v_2 = 0$, $v_d = v_1$ and v_o is proportional to the $-A_vv_1$. Thus, v_o is 180° out of phase (inverted) with respect to v_1. Similarly, if $v_1 = 0$, $v_d = -v_2$ and v_o is proportional to $+A_vv_2$ and the input and output are in phase (non-inverted).

Usually two constant supplies, one positive and one negative, are used to bias the Op-amp and connections to them are indicated by the dashed lines in Fig. 4.3a. Implied by this representation is that the second terminal of the bias source is connected to ground. Thus, the terminal labeled $+V_{bias1}(-V_{bias2})$ signifies connection to a positive (negative) supply with the negative (positive) supply terminal grounded. This is illustrated in Fig. 4.4. Note that these bias sources do not appear in the model in Fig. 4.3b. The equivalent circuit is used *only* to relate the output and input *signals*. It is assumed that the Op-amp operates on the linear segment of its voltage transfer characteristic (VTC) with the output range limited by the bias supplies. This is indicated in the VTC in Fig. 4.5 where the maximum positive and negative values of v_o are limited by $+V_{bias1}$ and $-V_{bias2}$. The Op-amp is said to be saturated once the bias supplies limit v_o. That is, for $v_d > v_A$, $v_o = -V_{bias2}$ and for $|v_d| > v_B$, $v_o = +V_{bias1}$. Along the horizontal portions of the VTC, v_o is not proportional to v_d and operation is non-linear. Observe that $v_d > 0$ ($v_1 > v_2$) causes $v_o < 0$ and visa versa indicating the inverting and non-inverting behavior of v_o relative to v_d. Along the linear segment

of the VTC the magnitude of the slope is the value of A_v which is called the *open-loop gain*. In commercial Op-amps, A_v is usually specified in volts per millivolt (V/mV) with $A_v > 50V/mV$ typical. Since an Op-amp is a voltage-controlled voltage source we expect R_i to be "large" and R_o to be "small". Common ranges for these quantities in commercially available Op-amps are $1M\Omega \leq R_i \leq 10^6 M\Omega$ and $25\Omega \leq R_o \leq 250\Omega$. Consequently, we expect currents entering the + and - inputs to be extremely small (from fractions of pA to a few tens of nA). Similarly, the expected voltage drop across the low-valued R_o is very small compared to $A_v v_d$.

The following examples illustrate the effect of the non-ideal nature of this voltage-controlled voltage source.

Example 4.1

The Op-amp stage in Fig. 4.6 has $A_v = 100\,\text{V/mV}$ (10^5), $R_i \to \infty$, $R_o = 0$, $R_1 = 1\,\text{k}\Omega$ and $R_2 = 10\,\text{k}\Omega$. Evaluate $A_V = v_o/v_s$.

Solution: The equivalent circuit of the stage, based on the model in Fig. 4.3b is displayed in Fig. 4.7. Note that external elements are drawn in black and the Op-amp equivalent is drawn in blue.

$$v_o = -A_v v_d \tag{1}$$

In a clockwise direction

$$v_d = iR_2 + v_o \tag{2}$$

Substitution of (1) into (2), combining terms and solving for l yields

$$i = \frac{v_d(1 + A_v)}{R_2} \tag{3}$$

In a counter-clockwise direction

$$v_d = -iR_1 + v_s$$

from which

$$i = (v_s - v_d)/R_1 \tag{4}$$

Equating (3) and (4) and solving for v_d gives

$$v_d = \frac{R_2 v_s}{R_2 + (1 + A_v)R_1} \tag{5}$$

Substitution of (5) and (1) and forming $A_V = v_o/v_s$ results in

$$A_V = \frac{-R_2 A_v}{R_2 + (1 + A_v)R_1}$$

Use of the given numerical values and carrying the results to four significant figures gives

$$\boxed{A_V = -9.999}$$

Example 4.2

Repeat Ex. 4.1 except $R_i = 5\,\text{M}\Omega$.

Solution: The model for the stage is shown in Fig. 4.8a. Obtaining a Thèvenin equivalent for the portion of the circuit to the left of X-X results in the circuit depicted in Fig. 4.8b where

$$V_{TH} = \frac{R_i}{R_1 + R_i} v_s \quad R_{TH} = R_1 || R_i = \frac{R_1 R_i}{R_1 + R_i}$$

Comparison of Figs. 4.8b and 4.7 indicate they are the same. Thus, from (5) in Ex. 4.1,

$$v_d = \frac{R_2 V_{TH}}{R_2 + (1 + A_v) R_{TH}} = \frac{R_2}{R_2 + [(1 + A_v) R_1 R_i / (R_1 + R_i)]} \times \frac{R_i v_s}{R_1 + R_i}$$

Evaluating v_d yields

$$v_d = 0.9990 \times 10^{-4} v_s$$

resulting in

$$A_V = -10^5 \times 0.9990 \times 10^{-4} \quad \text{and} \quad \boxed{A_V = -9.990}$$

Note that this result deviates from that in Ex. 4.1 by less than 0.1 percent.

Example 4.3

Repeat Ex. 4.1 except $R_o = 100\,\Omega$.

Solution: Figure 4.9 is the equivalent circuit of the stage. The output is

$$v_o = i R_o - A_v v_d \tag{1}$$

KVL for the loop is

$$-v_s + i R_1 + i R_2 + i R_o - A_v v_s = 0 \tag{2}$$

In a counter-clockwise direction

$$v_d = -R_1 i + v_s \tag{3}$$

Substitution of (3) into (2) and solving for i yields

$$i = \frac{v_s (1 + A_v)}{R_1 (1 + A_v) + R_2 + R_o} \tag{4}$$

Use of (4) in conjunction with (3) gives v_d, after combining like terms, as

$$v_d = \frac{(R_2 + R_o) v_s}{R_1 (1 + A_v) + R_2 + R_o} \tag{5}$$

Substitution of (4) and (5) in (1) and solving for $A_V = v_o / v_s$ results in

$$A_V = \frac{-A_v R_2 + R_o}{R_1 (1 + A_v) + R_2 + R_o} \tag{6}$$

Evaluating (6) using the given numerical values yields

$$A_V = \frac{-10^5 \times 10^4 + 10^2}{10^3 (1 + 10^5) + 10^4 + 10^2} \quad \text{and} \quad \boxed{A_V = -9.999}$$

To four significant figures this result does not differ from A_V in Ex. 4.1.

Example 4.4

We now consider the Op-amp stage in Fig. 4.6 having the following parameters: $A_v = 10^5$, $R_i = 5M\Omega$ and $R_o = 100\Omega$. The external elements are: $v_s = 1.0$V, $R_1 = 1\text{k}\Omega$, and $R_2 = 10\text{k}\Omega$. Evaluate v_o, the gain of the stage $A_V = v_o/v_s$ and v_d.

Solution: First we construct an equivalent circuit of the stage using the model of the Op-amp of Fig. 4.3b. This is displayed in Fig. 4.10a in which the real, external elements are drawn in black while the elements of the model are drawn in blue. By evaluating v_d initially, we can evaluate all of the desired quantities. To accomplish this we convert v_s in series with R_1 and $A_v v_d$ in series with $R_o + R_2$ to their Norton equivalents depicted in Fig. 4.10b. The KCL equation at node v_d is

$$-\frac{v_s}{R_1} + \frac{v_d}{R_1} + \frac{v_d}{R_i} + \frac{v_d}{R_o + R_2} + \frac{A_v v_d}{R_o + R_2} = 0 \qquad (1)$$

Combining like terms allows (1) to be rewritten as

$$v_d \left[\frac{1}{R_1} + \frac{1}{R_i} + \frac{(1 + A_v)}{R_o + R_2}\right] = \frac{v_s}{R_1} \qquad (2)$$

Solving for v_d yields, after some algebra,

$$v_d = \frac{R_i(R_o + R_2)v_s}{(R_1 + R_i)(R_o + R_2) + (1 + A_v)R_1 R_i} \qquad (3)$$

Evaluating v_d results in

$$v_d = \frac{5 \times 10^6(0.1 \times 10^3 + 10 \times 10^3) \times 1.0}{(10^3 + 5 \times 10^6)(0.1 \times 10^3 + 10 \times 10^3) + (1 + 10^5) \times 10^3 \times 5 \times 10^6}$$

from which

$$\boxed{v_d \simeq 101.0\mu V}$$

We can rewrite the KCL equation at node v_d as

$$\frac{v_d - v_s}{R_1} + \frac{v_d}{R_i} + \frac{v_d - v_o}{R_2} = 0 \qquad (4)$$

Solving for v_o after combining like terms and multiplying through by R_2 gives

$$v_o = v_d \left[\frac{R_2}{R_i} + \frac{R_2}{R_1}\right] - \frac{R_2}{R_1} v_s \qquad (5)$$

Substitution of values results in

$$v_o = 101 \times 10^{-6} \left[\frac{10 \times 10^3}{5 \times 10^6} + \frac{10 \times 10^3}{10^3}\right] - \frac{10 \times 10^3}{10^3} \times 1.0$$

from which, to four significant figures,

$$\boxed{v_o = -9.999V}$$

The gain A_V is then

$$A_V = \frac{v_o}{v_s} = \frac{-9.999}{1.0} \quad \text{and} \quad \boxed{A_V = -9.999}$$

The numerical values of the Op-amp parameters in Ex. 4.4 are typical of those commercially available. Inspection of these values make is obvious that $A_v >> 1$ and R_i is much larger than any other resistance in the circuit. If we make those approximations in (3) and (5), we could obtain the same values to three and perhaps four significant figures.

Example 4.5

Determine A_V for the circuit of Fig. 4.6 for the following parameter values: $A_V = 5\times10^4$, $R_i = 1M\Omega$ and $R_o = 200\Omega$. The values of v_s, R_1 and R_2 are given in Ex. 4.4.

Solution: We have selected "worst-case" parameter values. That is A_v and R_i are significantly lower while R_o is at its largest extreme. We will evaluate A_V to four significant figures to highlight the difference between this value and the one obtained in Ex. 4.4. Again, we use (3) and (5) in Ex. 4.4. After substitution of values

$$v_d = \frac{10^6(0.2\times10^3 + 10\times10^3)\times 1.0}{(10^3+10^6)(0.2\times10^3+10\times10^3)+(1+5\times10^4)10^3\times10^6} = 0.204mV$$

$$v_o = 0.204\times10^(-3)\left[\frac{10^4}{10^6}+\frac{10^4}{10^3}\right] - \frac{10^4}{10^3}\times 1.0 = -9.998V$$

$$A_V = \frac{v_o}{v_s} = \frac{-9.998}{1.0} \quad \text{and} \quad \boxed{A_V = -9.998}$$

The result in Ex. 4.5 nearly identical to that in Ex. 4.4. The parameter values in Ex. 4.5 differ by at least 50% from those in Ex. 4.4. Yet despite such gross changes, the A_V values differ by only one part per 10^4. Indeed, to three significant figures $A_V = -10.0$. The underlying reason for such precision is *feedback*[2]. Feedback is a self-regulating process that is ubiquitous in both the natural and man-made worlds. It is what maintains our body temperature at a nominal $37°C$, it is the basis of what we refer to as the "balance of nature", it helps us drive our automobiles at constant speed and is the mechanism by which the radar antenna at an airport rotates at constant angular velocity.

To illustrate the feedback process, consider driving a car at constant speed on a level road. (No cruise control is allowed!) The speed of the car is proportional to the displacement of the accelerator pedal from its rest position. Once in motion the driver samples the speedometer. If the speed is too high or too low, the driver adjusts the position of the accelerator petal appropriately. At the desired speed, no adjustments are needed. Notice that to regulate the speed, the driver needs to know what the speed is, otherwise no correction is possible. In essence, the output (the speed) depends, in part, on the value of the output. This paradoxical statement is a key feature of feedback systems.

[2]Harold Black's inspiration for his invention/discovery of the feedback amplifier came on the ferry he boarded in Weehauken, NJ and terminated not far from where he worked at Bell Telephone Laboratories on West Street in Manhattan's Greenwich Village. His initial derivations and calculations were done on a blank portion of a page in the New York Times. Distortion and performance variations introduced by manufacturing tolerances were significant problems facing the engineers designing long distance telephone systems in 1927. Their difficulties were compounded because the vacuum tubes used (the controlled sources of the period) did not always provide sufficient gain and often had unacceptable unit-to-unit variation. Because the benefits of feedback required a gain reduction, as we observed with $A_v = 10^5$ and $|A_V| = 10$ in Ex. 4.4, colleagues reaction could not have been worse. This reaction culminated when Dr. Arnold, the director of Bell Labs, forbade Black from continuing his work on feedback. Fortunately, Harry Nyquist and Hendryk Bode (pronounced Bó-deh), two of ECE's icons, saw sufficient merit in the concept to warrant further investigation. Working with Black they demonstrated feedback's efficacy both experimentally and theoretically. Since then a case could be made that the myriad of new circuits developed in the 1930s and 1940s violated Black's extensive patent disclosure on the use of feedback.

The same process exists in the Op-amp stage in Fig. 4.10. To simplify our discussion let us assume $R_o = 0$ which makes $v_o = -A_v v_d$. (See Fig. 4.8a and Ex. 4.2) But $v_d = i_N R_i$ and $i_N = i_1 - i_2$ where $i_2 = (v_d - v_o)/R_2$ and $i_1 \approx (v_s - v_d)/R_1$. Since v_o is phase inverted, i.e., a positive v_s produces a negative v_o, we can express i_2 as

$$i_2 = \frac{v_d + |v_o|}{R_2} \tag{4.2}$$

Thus, as $|v_o|$ tends to become larger (smaller) than a desired value, i_2 increases (decreases) causing i_N to decrease (increase). Consequently v_d decreases (increases) and $|v_o|$ decreases (increases) towards its desired value illustrating the self-regulation of the circuit. Feedback, in modern ECE, is what allows us to build systems having precision performance with imprecise components that display $\pm 10\%$ and often higher variations. How many of us would purchase an automobile if most of the 5,000 or so parts such as doors and axles had $\pm 10\%$ tolerance?

4.3 The Ideal Operational Amplifier

The VTC of a 741-type Op-amp[3] biased by ± 15V sources is displayed in Fig. 4.11a. Note the v_o and v_d are plotted in volts and millivolts, respectively. The open-loop gain A_v is the magnitude of the slope in the linear portion of the VTC and is $A_v = |(15-0)/(0-0.75)|$ and $A_v = 200V/mV = 200,000$. Let us replot Fig. 4.11a with both v_o and v_d given in volts. The resultant VTC is shown in Fig. 4.11b for which it appears that A_v is infinite and $v_d = 0$. A consequence of $v_d = 0$ is that $v_1 = v_2$, i.e., the voltages at the inverting and non-inverting terminals are equal. It is important to remember that although $A_v \to \infty$, the output remains finite and it limited by the supply voltages[4].

In the previous section we demonstrated that the voltage drop across R_o is a small fraction of v_o. Thus, if we assume $R_o \approx 0$, the effect on v_o is negligible. Two consequences arise because R_i is very large and significantly larger than any other resistance used. First is that the current in R_i is very small and negligible compared to the currents in the external elements. Since R_i is connected between the inverting and non-inverting terminals, the current entering those terminals is also negligible. Second, the series combination of any resistance in the stage and R_i is essentially R_i while the parallel combination with R_i is the other resistance. Why?

The statements in the two prior paragraphs lead to an idealization of physical Op-amps. This ideal Op-amp simplifies the analysis of circuits containing real Op-amps and provides accurate results that are extremely useful in design. To distinguish ideal Op-amps from real ones, the inside of the triangular circuit symbol is shaded as depicted in Fig. 4.12. This differentiation is used throughout the text. The properties of the ideal Op-amp are summarized as follows:

(1) The open-loop gain A_v is infinite.

(2) The difference voltage $v_d = 0$ so that $v_1 = v_2$.

(3) The input resistance R_i is infinite (an open circuit) resulting in $i_N = i_P = 0$.

(4) The output resistance $R_o = 0$.

(5) The output voltage v_o is finite.

In the next section we introduce two basic Op-amp stages which demonstrate how the properties of ideal Op-amps are used in analysis and design.

[3]The 741-type is among the most widely used Op-amps since its introduction in the late 1960s. Currently, several manufacturers fabricate 741-type Op-amps.

[4]In practice, the limiting voltages are often slightly less than the supply voltages.

4.4 Inverting and Non-Inverting Amplifiers

The circuit in Fig. 4.13 is an *inverting amplifier* stage utilizing an ideal Op-amp.. Since $i_N = 0$, (property 3), KCL at the junction of R_1 and R_2 yields $i_1 = i_2$. With $v_d = 0$ (property 2),

$$i_1 = \frac{v_s - 0}{R_1} = \frac{v_s}{R_1} \tag{4.3}$$

$$i_2 = \frac{0 - v_o}{R_2} = -\frac{v_o}{R_2} \tag{4.4}$$

Equating i_1 and i_2 and solving for the gain $A_V = v_o/v_s$ results in

$$A_V = \frac{v_o}{v_s} = -\frac{R_2}{R_1} \tag{4.5}$$

Two important observations arise from Eq. 4.5. The first is that A_V depends only on the resistance ratio. In the fabrication of ICs, resistance ratios can be controlled with greater precision than the values of individual resisitances[5]. Secondly, A_V depends on element values that are *external to the amplifying device.* Thus, the circuit designer can achieve the gain and precision required by controlling the resistances used.

Example 4.6

The circuit in Fig. 4.13 is designed with $R_1 = 1\text{k}\Omega$ and $R_2 = 10\text{k}\Omega$.

(a) Evaluate the gain A_V.

(b) For $v_s = 100mV$, determine v_o, i_1 and i_2.

(c) Compare the results in (a) and (b) with those in Ex. 4.4b.

Solution:

(a) From Eq. 4.5

$$\boxed{A_V = -\frac{10\text{k}\Omega}{1\text{k}\Omega} = -10}$$

(b) From, $A_V = v_o/v_s$,

$$\boxed{v_o = A_V v_s = -10 \times 0.1 = -1.0V}$$

Use of Eqs. 4.3 and 4.4 yield

$$\boxed{i_1 = \frac{100mV}{1\text{k}\Omega} = 100\mu A} \qquad \boxed{i_2 = -\frac{-1.0V}{10\text{k}\Omega} = 100\mu A}$$

(c) In Ex. 4.4, the corresponding values are: $A_V = -9.999$, $v_o = -0.9999V$ as given, $i_1 = i_2 = 99.99\mu A$. The results using the ideal and typical non-ideal Op-amps differ by one part in 10^4, i.e., by 0.01%. Clearly, analysis and design with the ideal Op-amps is simpler, more efficient and gives accurate results.

[5]The ratio of discrete resistors is limited by the manufacturing accuracy of the individual resistances. Thus, for $\pm 5\%$ tolerances, R_1/R_2 has a worst-case deviation of $\pm 10\%$. For an IC this ratio is often less than 1%.

Example 4.7

Design an inverting amplifier stage that provides 1.0V output for a 25mV input. The current in R_1 and R_2 cannot exceed $50\mu A$ and the largest allowable resistance value is 30kΩ.
Solution: The required resistance ratio from Eq. 4.5 is

$$|A_V| = \left|\frac{v_o}{v_s}\right| = \frac{1.0\text{V}}{25mV} = \frac{R_2}{R_1} \text{and} \frac{R_2}{R_1} = 40$$

If we choose $R_2 = 30\text{k}\Omega$, the largest permissible value $R_1 = \frac{30\text{k}\Omega}{40} = 0.75\text{k}\Omega$. The current in R_1 is, using Eq. 4.3

$$i_1 = \frac{25mV}{0.75\text{k}\Omega} = 33.3\mu A$$

Since $i_1 = i_2$, these resistance values satisfy the current specification. Alternatively, we can select R_1 to satisfy the maximum current allowed. Thus, from Eq. 4.3,

$$R_1 = \frac{25mV}{50\mu A} = 0.5\text{k}\Omega \qquad \text{which makes} \qquad R_2 = 40 \times 0.5\text{k}\Omega = 20\text{k}\Omega$$

The design will satisfy all the specifications provided $R_2/R_1 = 40$ and

$$\boxed{0.5\text{k}\Omega \leq R_1 \leq 0.75\text{k}\Omega} \qquad \boxed{20\text{k}\Omega \leq R_2 \leq 30\text{k}\Omega}$$

The designer in Ex. 4.7 must select R_1 and R_2 from a range of allowable values. Other performance and fabrication factors usually influence the values used. For example, if we wish to minimize power dissipation in R_1 and R_2 we select the largest values possible. Power is $i_1^2(R_1+R_2)$ as $i_1 = i_2$; larger resistance values cause i_1^2 to decrease faster than $(R_1 + R_2)$ increases. In IC design, chip area is often at a premium. The area needed to fabricate a resistor is proportional to the resistance value. Thus, if power is not as critical a factor, the choice is the smallest resistance values.

The Op-amp in Fig. 4.14a is used in a *non-inverting amplifier stage.* An alternate schematic for Fig. 4.14a is displayed in Fig. 4.14b. Analyzing the circuit in Fig. 4.14a, we observe that for $v_d = 0$ (property 2), the voltage at node N must be equal to v_s. Then,

$$i_1 = \frac{v_s}{R_1} \tag{4.6}$$

$$i_2 = \frac{v_o - v_s}{R_2} \tag{4.7}$$

Since $i_N = 0$ (property 3), KCL requires $i_1 = i_2$ or

$$\frac{v_s}{R_1} = \frac{v_o - v_s}{R_2} \tag{4.8}$$

Solving Eq. 4.8 for v_o/v_s yields

$$A_V = \frac{v_o}{v_s} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \tag{4.9}$$

Equation 4.9 indicates that A_V depends on the resistance ratio. Thus, the gains of both the non-inverting and inverting stages depend only on R_2/R_1.

Example 4.8

Design the amplifier in Ex 4.7 as a non-inverting stage.
Solution: From Ex. 4.7, $A_V = 40$ and use of Eq. 4.9 gives

$$40 = 1 + \frac{R_2}{R_1} \text{or} \frac{R_2}{R_1} = 39$$

Selecting $R_2 = 30\text{k}\Omega$ results in $R_1 = \frac{30\text{k}\Omega}{39} = 0.769\text{k}\Omega$. From Eq. 4.6, $i_1 = \frac{25mV}{0.769\text{k}\Omega} = 32.5\mu A$ which easily satisfies the allowable current requirement. If we choose R_1 to just meet the maximum current, then

$$i_1 = 50\mu A = \frac{25mV}{R_1} \quad \text{or} \quad R_1 = \frac{25mV}{50\mu A} = 0.5\text{k}\Omega \quad R_2 = 39 \times 0.5 = 19.5\text{k}\Omega$$

Therefore, provided $R_2/R_1 = 39$, the ranges are

$$\boxed{0.5\text{k}\Omega \leq R_1 \leq 0.769\text{k}\Omega} \qquad \boxed{19.5\text{k}\Omega \leq R_2 \leq 30\text{k}\Omega}$$

If $R_2 = 0$ in Fig. 4.14a, use of Eq. 4.9 results in $A_V = 1$ and R_1 is unnecessary. Shown in Fig. 4.15, this stage is called a *voltage-follower* or *unity-gain buffer*. With infinite input resistance, zero output resistance and unity gain, the voltage-follower's performance is similar to the emitter-follower described in Exs. 3.19 and 3.20 in Sec. 3.5. Amplifiers must operate linearly if they are to faithfully reproduce the input signal. Consequently, the saturation values of v_o limit the input voltage range that can be accommodated in an Op-amp stage. For the inverting stage,

$$\frac{V_{bias1}}{A_V} \leq v_s \leq -\frac{V_{bias2}}{A_V} \qquad (a) \tag{4.10}$$

and for non-inverting stages

$$-\frac{V_{bias2}}{A_V} \leq v_s \leq \frac{V_{bias1}}{A_V} \qquad (b)$$

Example 4.9

An Op-amp is biased with ± 10V supplies and uses $R_1 = 1.5\text{k}\Omega$ and $R_2 = 6.0\text{k}\Omega$. What range of input signals can be processed linearly in an

(a) inverting stage and

(b) a non-inverting stage?

Solution:

(a) For an inverting stage $A_V = -R_2/R_1$ so that $A_V = -6.0\text{k}\Omega/1.5\text{k}\Omega = -4$. Use of Eq. 4.10a gives

$$\frac{10}{-4} \leq v_s \leq \frac{-10}{-4} \quad \text{or} \quad \boxed{-2.5V \leq v_s \leq +2.5V}$$

(b) A_V for the non-inverting stage is $(1 + R_2/R_1) = 1 + 4 = 5$. Then, from Eq. 4.10b,

$$\frac{-10}{5} \leq v_s \leq \frac{+10}{5} \quad \text{or} \quad \boxed{-2V \leq v_s \leq +2V}$$

Inverting and non-inverting stages are the basis for a variety of circuits that perform mathematical functions. In the next few sections, we demonstrate several such applications.

4.5 Difference and Summing Circuits

The circuit shown in Fig. 4.16a is a difference amplifier whose output v_o is expressed as $av_2 - bv_1$. The terminals labeled v_1 and v_2 indicate that one terminal of a signal source is connected to it while the unseen terminal is at ground. To verify the previous statement, we first thèvenize[6] the portion of the circuit enclosed by the rectangle in Fig. 4.16a containing v_s, R_3 and R_4. The Thèvenin voltage V_{TH} is given by the voltage-divider relation as

$$V_{TH} = \frac{R_4}{R_3 + R_4} v_2 \tag{4.11}$$

The Thèvenin resistance R_{TH} is

$$R_{TH} = R_3 \parallel R_4 = \frac{R_3 R_4}{R_3 + R_4} \tag{4.12}$$

The Thèvenized circuit is shown in Fig. 4.16b and analysis proceeds using superposition.

First suppress V_{TH} as displayed in Fig. 4.17a. This results in an inverting stage since the non-inverting terminal is at ground. No current exists in R_{TH} and, hence, the voltage across R_{TH} is zero. Then, v_{o1} is given by Eq. 4.5 as

$$v_{o1} = -\frac{R_2}{R_1} v_1 \tag{4.13}$$

Suppressing v_1 as depicted in Fig. 4.17b results in a non-inverting stage for which use of Eq. 4.9 yields

$$v_{o2} = \frac{R_1 + R_2}{R_1} V_{TH} \tag{4.14}$$

Substitution of Eq. 4.11 into Eq. 4.14 and forming $v_o = v_{o1} + v_{o2}$ gives

$$v_o = \frac{R_1 + R_2}{R_1} \times \frac{R_4}{R_3 + R_4} v_2 - \frac{R_2}{R_1} v_1 \tag{4.15}$$

Equation 4.15 verifies that $v_o = av_2 - bv_1$.

If we set $R_3 = R_1$ and $R_4 = R_2$, Eq. 4.14 reduces to

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) \tag{4.16}$$

The ratio R_2/R_1 allows the difference to be scaled; if $R_2 = R_1$, v_o is exactly equal to the difference of the inputs.

[6] Thèvenize is used as a verb to indicate that the thèvenized elements are to be replaced by their Thèvenin equivalent.

Example 4.10

Design a difference amplifier that provides $v_o = 3v_2 - 4v_1$. The signal sources v_1 and v_2 each have source resistances of 3kΩ.
Solution: From Eq. 4.15,

$$a = \frac{R_1 + R_2}{R_1} \times \frac{R_4}{R_3 + R_4} \qquad b = \frac{R_2}{R_1}$$

Each source resistance is in series with its signal source. Therefore we can choose to identify these resistances as R_1 and R_3. Thus,

$$\boxed{R_1 = 3\text{k}\Omega} \qquad \boxed{R_3 = 3\text{k}\Omega}$$

From b, $R_2 = bR_1 = 4 \times 3\text{k}\Omega$ and

$$\boxed{R_2 = 12\text{k}\Omega}$$

Substituting values into a results in

$$3 = \frac{3\text{k}\Omega + 12\text{k}\Omega}{3\text{k}\Omega} \times \frac{R_4}{3\text{k}\Omega + R_4}$$

Solving for R_4 yields

$$\boxed{R_4 = 4.5\text{k}\Omega}$$

An inverting summing amplifier is illustrated in Fig. 4.18. Because no current enters the Op-amp terminals (property 3), KCL at node A requires

$$i_R - i_1 - i_2 - i_3 - ... - i_N = 0 \qquad \text{or} \qquad i_R = i_1 + i + 2 + i_3 + ... + i_N \tag{4.17}$$

Since $v_d = 0$ (property 2) the voltage at node A is at ground and

$$i_1 = \frac{v_1}{R_1}, i_2 = \frac{v_2}{R_2}, i_3 = \frac{v_3}{R_3}, i_N = \frac{v_N}{R_N} \tag{4.18}$$

The current i_R in the feedback resistance R is

$$i_R = \frac{v_A - v_o}{R} = \frac{0 - v_o}{R} = \frac{-v_o}{R} \tag{4.19}$$

Substitution of Eqs. 4.18 and 4.19 into Eq. 4.17 and solving for v_o yields

$$v_o = -R\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + ... + \frac{v_N}{R_N}\right) \tag{4.20}$$

In Eq. 4.20 we observe that the resistances R_1, R_2, R_3...R_N can be used to scale the sum so that v_o is of the form

$$v_o = -(a_1 v_1 + a_2 v_2 + a_3 v_3 + ... a_N v_N) \tag{4.21}$$

When $R_1 = R_2 = R_3 = ... = R_N = R$, v_o becomes the sum of the input signals.

Example 4.11

The circuit in Fig. 4.19 is a 4-bit *binary weighted resistance digital-to-analog converter* (DAC). Each resistance is of the form $2^n \times 4\text{k}\Omega$ where n=0,1,2,3. Switches are closed or open when the corresponding bit is one or zero, respectively. Thus, S_3 is closed when the most significant bit (MSB) is one and open for an MSB of zero. Similarly, S_o is open or closed when the least significant bit (LSB) is zero or one, respectively.

For $V_R = 5\text{V}$ and $R = R_1 = 4\text{k}\Omega$, determine v_o when

(a) the MSB is one and all other bits are zero,

(b) the LSB id one and all other bits are zero, and

(c) all bits are one.

(d) Evaluate the conditions in (c) using SPICE.

Solution:

(a) An MSB of one closes S_3 and all other switches are open. Use of Eq. 4.19, after substitution of values, results in

$$v_o = -4\text{k}\Omega\left[\frac{-5}{4\text{k}\Omega} + 0 + 0 + 0\right] \quad \text{and} \quad \boxed{v_o = 5\text{V}}$$

(b) With S_o the only closed switch, Eq. 4.19 gives

$$v_o = -4\text{k}\Omega\left[0 + 0 + 0 + \frac{-5}{32\text{k}\Omega}\right] \quad \text{and} \quad \boxed{v_o = \frac{5}{8}\text{V} = 0.625\text{V}}$$

(c) When all switches are closed, Eq. 4.19 yields

$$v_o = -4\text{k}\Omega\left[\frac{-5}{4\text{k}\Omega} + \frac{-5}{8\text{k}\Omega} + \frac{-5}{16\text{k}\Omega} + \frac{-5}{32\text{k}\Omega}\right] \quad \text{and} \quad \boxed{v_o = 9.375\text{V}}$$

(d) The SPICE generated circuit is displayed in Fig. 4.20 and the netlist is given below.

```
                Circuit for Ex.4-11d
1:  *.OP
2:  V_V1          0  V1  10Vdc
3:  R_R1          V1  V2  2k
4:  R_R2          V1  V2  4k
5:  R_R3          V1  V2  8k
6:  R_R4          V1  V2  16k
7:  E_E1          V3  0  V2  0  1000000000000
8:  R_R5          V2  V3  1k
.END
```

Note that the output voltage v_o = V3 and its value is shown on Fig. 4.20. As expected it is the same as that calculated in part (c).

Also observe that SPICE cannot accommodate ideal Op-Amps. To approximate the ideal we selected A_v (E1 in the netlist) to be 10^{12}. This is so large that to four or five significant figures the results obtained are identical to those for an ideal Op-Amps.

If all of the voltages on the right side of Eq. 4.20 are equal to $-V_R$ and $R = R_1$ as they are in Ex. 4.11, Eq. 4.20 is expressible as

$$v_o = V_R\left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right) = V_R\left(\frac{1}{2^0} + \frac{1}{2^1} + \frac{1}{2^2} + \frac{1}{2^3}\right) \tag{4.22}$$

By increasing the number of bits, Eq. 4.22 becomes

$$v_o = V_R\left(\frac{1}{2^0}+\frac{1}{2^1}+\frac{1}{2^2}+\frac{1}{2^3}+...+\frac{1}{2^N}\right) = V_R\sum\frac{1}{2^n} \tag{4.23}$$

Since,

$$\lim_{n\to\infty}\sum_{n=0}^{N}\frac{1}{2^n} = 2, v_o \to 2V_R \tag{4.24}$$

Truncating the series causes v_o to differ from $2V_R$ by one LSB as is the case in Ex. 4.11.

Two practical limitations exist on how many bits this type of DAC can convert. The first is that the largest resistance used is frequently restricted by the fabrication processes. The second limits the size of the smallest resistance. As seen in Fig. 4.18, i_R is the output current of the Op-amp for which one constraint is power dissipation. Since $p = vi$, current is also constrained.

Example 4.12

A binary weighted resistance DAC is to be designed for which $V_R = 5$V, the maximum current is 80mA and all resistances $\leq$ 35kΩ. What is the maximum number of bits this DAC can convert?
Solution: With $V_R = 5$V, $v_o \approx 10$V [Eq. 4.24]. Therefore

$$R_{min} = \frac{v_o}{I_{max}} = \frac{10}{80mA} = 0.125\text{k}\Omega$$

All resistors in the DAC are of the form $2^n R_{min}$. For this case,

$$R_{max} \geq 2^n \times R_{min}$$

and

$$35\text{k}\Omega = 2^n \times 0.125\text{k}\Omega$$

from which

$$2^n = \frac{35\text{k}\Omega}{0.125\text{k}\Omega} = 280$$

Taking the logarithm of both sides and solving for n yields

$$n = \frac{log280}{log2} = 8.13$$

As n must be an integer we must choose the smaller integer so that $n = 8$. Note, even if n turned out to be 8.83, we would still have to choose $n = 8$ since $n = 9$ results in $R_{max} = 2^9 \times 0.125\text{k}\Omega = 64\text{k}\Omega$, whereas $n = 8$ gives $R_{max} = 32\text{k}\Omega$ which satisfies the specification.

The value of n is the largest value we can use. However, since the summation starts with $n = 0$, *the number of bits converted is nine*, i.e.,

$$n = 0, 1, 2, 3, 4, 5, 6, 7, 8$$

The corresponding resistances are:

$$0.125\text{k}\Omega, 0.25\text{k}\Omega, 0.50\text{k}\Omega, 1.00\text{k}\Omega, 2.00\text{k}\Omega, 4.00\text{k}\Omega, 8.00\text{k}\Omega, 16.0\text{k}\Omega, \text{and } 32.0\text{k}\Omega$$

The two constraints imposed by an ideal Op-amp–at the inverting and non-inverting inputs, no current exists and the voltages are equal–are the basis for analyzing circuits with several Op-amps. The following example serves as an illustration.

Example 4.13

Determine i_s in the circuit of Fig. 4.21 in terms of v_s and the circuit elements.
Solution: Both v_A and v_B are equal to v_s as the non-inverting terminals of both Op-amps are connected to the positive terminal of v_s. The portion of the circuit constrained within the dashed rectangle is a non-inverting amplifier whose gain, given by Eq. 4.9, is $1 + R/R = 2$. Therefore $v_{o1} = 2v_s$. The currents i_1 and i_2 are given by

$$i_1 = \frac{v_{o1} - v_B}{R_1} = \frac{2v_s - v_s}{R_1} = \frac{v_s}{R_1}; i_2 = \frac{v_s - V_{o2}}{R_2} \qquad (1)$$

Since no current enters the Op-amp, $i_2 = i_s$. Thus capacitor current i_c is

$$i_c = C\frac{d}{dt}(v_B - v_{o2}) = C\frac{d}{dt}(v_s - v_{o2}) \qquad (2)$$

KCL requires $i_1 = i_c$ so

$$\frac{v_s}{R_1} = C\frac{d}{dt}(v_s - v_{o2}) \qquad (3)$$

from which

$$C\frac{dv_{o2}}{dt} = C\frac{dv_s}{dt} - \frac{v_s}{R_1}$$

or

$$\frac{dv_{o2}}{dt} = \frac{dv_s}{dt} - \frac{v_s}{R_1C} \qquad (4)$$

Integrating both sides yields

$$v_{o2} = v_s - \frac{1}{R_1C}\int v_s dt \qquad (5)$$

Substituting for v_{o2} in (1) gives

$$i_2 = i_s = \frac{v_s}{R_2} - \frac{v_s}{R_2} + \frac{1}{R_1R_2C}\int v_s dt \quad \text{and} \quad \boxed{i_s = \frac{1}{R_1R_2C}\int v_s dt}$$

The circuit in Ex. 4.13 is an inductance simulator as indicated by the current being proportional to the integral of the voltage. Recall that $i_L = \frac{1}{L}\int v_L dt$ so the equivalent inductance is R_1R_2C. The significance of this result lies in the realization that inductors are extremely difficult to fabricate on integrated circuits. Those that are have values limited to about $1\mu H$ and are most often used at frequencies at or above tens of megahertz. This inductor simulator is capable of realizing inductors in the 1-50mH range and is useful at audio frequencies.

4.6 Integrators and Differentiators

We described circuits that added and subtracted signals in the previous section. Our focus now is on circuits that perform integration and differentiation. Figure 4.22 displays a simple integrator that incorporates an inverting Op-amp stage. In Fig. 4.22, node P is at ground because $v_d = 0$. Then,

$$i_R = \frac{v_s - 0}{R} = \frac{v_s}{R} \tag{4.25}$$

$$\text{and } i_C = C\frac{d}{dt}(0 - v_o) = -C\frac{dv_o}{dt} \tag{4.26}$$

KCL requires $-i_R + i_C = 0$ or $i_R = i_C$; combining Eqs. 4.25 and 4.26 gives

$$\frac{v_s}{R} = -C\frac{dv_o}{dt} \qquad \text{or} \qquad \frac{dv_o}{dt} = \frac{v_s}{RC} \tag{4.27}$$

Integrating both sides of Eq. 4.27 yields

$$v_o = \frac{-1}{RC}\int_0^t v_s d\tau \tag{4.28}$$

where τ is a dummy variable of integration. Usually, C is uncharged at $t = 0$ and $v_s(0)$ is finite making $v_o(0) = 0$. Thus, Eq. 4.27 verifies that v_o is the integral of v_s.

Example 4.14

The waveform in Fig. 4.23a is applied to the integrator in Fig. 4.22 with $RC = 1\mu s$. Sketch v_o.
Solution: For the first $0.5\mu s$, use of Eq. 4.28 gives the integrator output as

$$v_o = \frac{-1}{10^{-6}}\int_0^{0.5\times10^{-6}} 2dt = -2\times10^6 t\,|_0^{0.5\times10^{-6}} = -2\times10^6\times0.5\times10^{-6} = -1\text{V}$$

This equation shows that v_o is a linear function of time with a negative slope. At $t = 0.5\mu s$, the output becomes -1V. For $0.5\mu s \le t \le 1.0\mu s$,

$$v_o = \frac{-1}{10^{-6}}\int_{0.5\times10^{-6}}^{10^{-6}} -2dt = 2\times10^6 t|_{0.5\times10^{-6}}^{10^{-6}} = 2\times10^6\times[10^{-6} - 0.5\times10^6] = +1\text{V}$$

Since v_o is proportional to the area of the v_s curve, the total area for one cycle, is zero as the areas for each half-cycle are equal in magnitude but have opposite signs. Thus, the resultant waveform is as displayed in Fig. 4.23b.

Example 4.14 illustrates one method by which triangular waves are generated from square waves.

Interchanging R and C in Fig. 4.22 converts the circuit into a differentiator as shown in Fig. 4.24. Again, $v_d = 0$ so that

$$i_c = C\frac{dv_s}{dt} \qquad \text{and} \qquad i_R = \frac{-v_o}{R} \tag{4.29}$$

Since KCL requires $i_c = i_R$ (no current enters the Op-amp) using Eq. 4.29 to solve for v_o yields

$$v_o = -RC\frac{dv_s}{dt} \tag{4.30}$$

Example 4.15

For $RC = 1\mu s$ and v_s given by the waveform in Fig. 4.23b, sketch v_o for the differentiator in Fig. 4.24.
Solution: For $0 \leq t \leq 0.5\mu s$, the slope of the waveform is $-1/0.5\mu s = -2 \times 10^6$ which makes $v_s = -2 \times 10^6 t$. During this interval and using Eq. 4.30

$$(1) v_o = -10^{-6} \frac{d}{dt}(-2 \times 10^6 t) = -10^{-6} \times (-2 \times 10^6) = 2\text{V}$$

For times between $0.5\mu s$ and $1.0\mu s$, the slope of the waveform is the negative of that for $0 \leq t \leq 0.5\mu s$. Consequently, v_o is just negative of that given in (1) or $v_o = -2$V. Since v_s is periodic, these results repeat for each cycle of $1\mu s$. The resultant sketch of v_o is displayed in Fig.4.25.

As expected the result in Ex. 4.15 is the original waveform in Fig. 4.23a and Ex. 4.14.

4.7 Log and Antilog Amplifiers

Log and antilog circuits find use in a number of instrumentation systems where the data must be transmitted from where measurement occurs to where it is recorded and processed. Their use is often necessitated because the data spans four or five orders of magnitude. The range of signals from largest to smallest that a circuit processes is referred to as its *dynamic range*. Thus, if the smallest signal is 0.1mV and the largest is 10V, a circuit must have a dynamic range of 10^5,i.e., five orders of magnitude. Since most data is transmitted digitally, we need at least 17 bits to represent all of the data. What a logarithm does is compress the span of values, e.g., for a range from 1 to 10^5, the corresponding range of logarithms is from zero to five. This results in fewer bits transmitted with reconstruction of the original data (the antilog) occurring at the site where data is processed.

The elementary amplifier in Fig. 4.26 contains a semiconductor diode in the feedback loop. While diodes have many practical applications, in this circuit it behaves as a non-linear resistance for which, $v_D > 0$,

$$i_D = I_s \varepsilon^{v_D/V_T} \tag{4.31}$$

When $v_s > 0$, $v_o < 0$ since this is an inverting stage. Since $v_d = 0$, $V_N = 0$ and the current entering the Op-amp is zero, the currents are

$$i_R = \frac{v_s}{R} \tag{4.32}$$

and

$$i_D = I_s \varepsilon^{(0-v_o)/V_T} \tag{4.33}$$

Since $v_o < 0$, Eq. 4.33 may be rewritten as

$$i_D = I_s \varepsilon^{|v_o|/V_T} \tag{4.34}$$

Equating i_D and i_R (from KCL at node N) we obtain

$$\frac{v_s}{R} = I_s \varepsilon^{|v_o|/V_T} \quad \text{or} \quad \varepsilon^{|v_o|/V_T} = \frac{v_s}{RI_s} \tag{4.35}$$

Taking the natural log of each side in Eq. 4.35 and then solving for v_o results in

$$|v_o| = V_T \ln \frac{v_s}{RI_s} \tag{4.36}$$

Thus, this circuit behaves as a *log amplifier*.

Example 4.16

Determine the range for v_o in the log amplifier in Fig. 4.26 for $0.1mV \leq v_s \leq 10V$. The parameter values are $R = 1\text{k}\Omega$, $V_T = 25mV$, and $I_s = 10^{-16}A$.
Solution: Substitution of values into Eq. 4.35 yields

$$|v_o| = 25 \times 10^{-3} \ln \frac{v_s}{10^3 \times 10^{-16}} = 25 \times 10^{-3} \ln 10^{13} v_s$$

For $v_s = 0.1mV$, $|v_o| = 0.518V$; when $v_s = 10V$, $|v_o| = 0.806V$. Thus the range of $|v_o|$ values is

$$\boxed{0.518 \leq |v_o| \leq 0.806V}$$

Observe how a dynamic range of 10^5 translates to less than one-half order of magnitude on a logarithm scale.

The antilog amplifier is constructed by interchanging the diode and resistance in Fig. 4.26 as shown in Fig. 4.27. Following the analysis of the log amplifier, $i_D = i_R$ and $v_D = v_N = 0$. Thus,

$$I_s \varepsilon^{v_s/V_T} = |v_o|/R \tag{4.37}$$

and

$$|v_o| = I_s R \ln^{-1}\left(\frac{v_s}{V_T}\right) \tag{4.38}$$

Equation 4.38 uses the fact that exponentiation is the inverse of taking the logarithm.

Example 4.17

For $0.518 \leq v_s \leq 0.806V$, determine the range of values for $|v_o|$ for the antilog amplifier in Fig. 4.27. The parameter values are: $R = 1\text{k}\Omega$, $I_s = 10^{-16}A$ and $V_T = 25mV$.
Solution: Substitution of values into Eq. 4.33 yields

$$|v_o| = 10^{-16} \times 10^3 \ln^{-1}\left(\frac{v_s}{25 \times 10^{-13}}\right)$$

For $v_s = 0.518$, evaluation of (1) gives $|v_o| = 0.0997mV$; with $v_s = 0.806$ we obtain $|v_o| = 10.04V$. Therefore, the range of values is

$$0.0997mV \leq |v_o| \leq 10.04V$$

The values of v_s in Ex. 4.17 are the values of $|v_o|$ obtained in Ex. 4.16 for the log amplifier. The output of the antilog amplifier in Ex. 4.17 is the input range in Ex. 4.16 with slight differences due to roundoff error. This pair of examples demonstrate that the compressed dynamic range of the log amplifier and the ability to the antilog amplifier to reconstitute the original signals.

Using real rather than ideal Op-amps in the circuits of Figs. 4.26 and 4.27 causes their performance to deviate from that given by in Eqs. 4.36 and 4.38. In addition, manufacturing and environmental

variations of component values further deteriorates performance. Consequently, practical log and antilog amplifiers contain additional circuitry to mitigate the effects of these variations.

Example 4.18

Determine v_o for the system described by the block diagram in Fig. 4.28.
Solution: The output of each log amplifier is proportional to the natural log of the input and K is the constant of proportionality. Therefore, $v_{01} = -K \ln v_1$ and $v_{02} = -K \ln v_2$. (Recall that $v_o < 0$ in Fig. 4.26.) The inverting unity gain summer has an output equal to the negative of the sum of the inputs so

$$v_{03} = K \ln v_1 + K \ln v_2 = K[\ln v_1 + \ln v_2]$$

Recall the sum of logarithms corresponds to multiplication. Thus,

$$v_{03} = K \ln(v_1 v_2)$$

The antilog amplifier's constant of proportionality is $1/K$ which makes

$$v_o = \frac{1}{K} \ln^{-1} v_{03} \qquad \text{and} \qquad \boxed{v_o = v_1 v_2}$$

The circuit analyzed in Ex. 4.18 functions as an analog multiplier. In Sec. 4.8 we introduce analog multipliers and several of its applications. Note that to achieve multiplication a non-linear element must be present since multiplication is not a linear operation.

4.8 Analog Multiplier Applications

Analog multipliers are commercially available ICs whose design is based on the behavior of transistors rather than log amplifiers. The circuit symbol is given in Fig. 4.29 and, as expressed in Eq. 4.39, indicates its output is proportional to the product of the pair of inputs.

$$v_o = \frac{v_1 v_2}{K} \tag{4.39}$$

The rationale for expressing the constant of proportionality as 1/K is because it is desirable that v_1, v_2 and v_o have the same range of values. Thus, if $-10V \leq v_1 \leq +10V$ and $-10V \leq v_2 \leq +10V$, choosing $K = 10V$ results in $-10V \leq v_o \leq +10V$. Note that K has the dimension volts.

Example 4.19

The input to a multiplier with $K = 10V$ are two square waves. The waveform for v_1 is shown in Fig. 4.30a. For each v_2 given in Figs. 4.30b,c,d, sketch v_o.

Solution: The v_2 given in Fig. 4.30b is identical to that for v_1,i.e., they are in phase. Thus, both waveforms are either positive or negative during the same intervals of time. Use of Eq. 4.39 results in the waveform given in Fig. 4.31a. The waveform in Fig. 4.30c is 180° out of phase with v_1 so the product $v_1 v_2$ is always a negative constant as displayed in Fig. 4.31b.

The waveform in Fig. 4.30d is out of phase with v_1 by one-quarter of a cycle or 90°. During the interval $0 \leq t \leq T/4$ both v_1 and v_2 are positive; for $T/4 \leq t \leq T/2$, v_2 is negative and v_1 remains positive. During the second half-cycle, v_1 and v_2 are both negative for $T/2 \leq t \leq 3T/4$. At $t = 3T/4$, v_2 becomes positive with v_1 remaining negative. The resultant output is displayed in Fig. 4.31c.

In Fig. 4.31 we observe that the amount of time per cycle v_o is negative is an indicator of the phase difference between v_1 and v_2. When they are 180° out of phase v_o is always negative and for a 90° phase difference, v_o is negative for one-half cycle. Multipliers used in this application are called *phase detectors* which are essential features of *automatic frequency control* (AFC) in communications and the clock generators in digital systems.

The circuit shown in Fig. 4.32 illustrates how the multiplier is used as a *divider circuit*,i.e., one that performs algebraic division. The multiplier output from Eq. 4.39 is $v_A = v_o v_2/K$. Both v_N and i_N are zero; therefore, KCL dictates $i_1 = i_2$ where $i_1 = v_s/R_1$ and $i_2 = (0 - v_A)/R_2 = -v_o v_2/KR_2$. Equating i_1 and i_2 and solving for v_o yields

$$v_o = -\frac{KR_2}{R_1} \times \frac{v_1}{v_2} \tag{4.40}$$

Example 4.20

In the circuit of Fig. 4.32, $K = 10V$, $R_1 = 10\text{k}\Omega$, $R_2 = 5\text{k}\Omega$, $v_1 = 2\sin\omega t$ and $v_2 = 4\cos\omega t$. Determine v_o.

Solution: Substitution of values into Eq. 4.40 yields

$$v_o = -\frac{10 \times 5\text{k}\Omega}{10\text{k}\Omega} \times \frac{2\sin\omega t}{4\cos\omega t}$$

Recognizing that $\sin x/\cos x = \tan x$, the output is

$$\boxed{v_o = -2.5\tan\omega t}$$

The result in Ex. 4.20 demonstrates that trigonometric functions can also be generated.

Connecting the two multiplier inputs as shown in Fig. 4.33 produces an output proportional to the input squared. This circuit is used in the *square-root circuit* of Fig. 4.34. The voltage $v_A = v_o^2/K$ and $v_N = 0$ since $v_N = v_P$ and v_P is at ground. KCL at node N requires $i_1 = i_2$ as $i_N = 0$. Then, $i_1 = v_s/R_1$ and $i_2 = (v_N - v_A)/R_2 = -v_o^2/KR_2$. Equating i_1 and i_2 and solving for v_o results in

$$v_o = \sqrt{-\frac{KR_2}{R_1}v_s} \tag{4.41}$$

Since the quantity inside the radical must be positive, *Eq. 4.41 is valid only for* $v_s < 0$.

This completes our discussion of how Op-amps in conjunction with analog multipliers are able to perform a wide variety of mathematical operations.

4.9 SPICE Models of Operational Amplifiers

The equivalent circuit in Fig. 4.3b of a practical Op-amp is readily accommodated in SPICE. However, an ideal Op-amp cannot be modeled as $A_v \to \infty$ and $R_i \to \infty$ are not allowed by SPICE. Consequently, ideal Op-amps must be represented by non-ideal ones. The values of the parameters in the non-ideal model are selected to give the same results as obtained when ideal Op-amps are used. To approximate ideal behavior the circuit in Fig. 4.35 may be used with the following parameter constraints:

1. R_i is made very much larger than any other resistance in the circuit. Usually, $R_i \geq 10^8\,\Omega$ suffices.
2. $A_v \geq 10^6$ generally provides the same results as if $A_v \to \infty$.
3. R_o is selected to be much smaller than any other circuit resistance. Typically, $R_o \leq 1\,\Omega$ suffices to give ideal results.

Note that in Ex. 4-11, Fig. 4.20 is similar to the SPICE version of Fig. 4.19 for which $A_v = 10^{12}$, $R_i \to \infty$ and $R_o \to 0$. Selecting $R_i \to \infty$ was allowed because of the resistances connected to it. Similarly, $R_o = 0$ is used because the output is taken directly across the Op-amp and no current exists in the external terminals.

Example 4.21

Determine the output voltage for the difference amplifier shown in Fig. 4.36a using SPICE.

Solution: The SPICE generated circuit is displayed in Fig. 4.36b. The Netlist is as follows

```
 1:  Circuit for Ex.4-21
 2:  V_V1        V1  0   1Vdc
 3:  R_R1        V1 V2     1k
 4:  R_R2        V2  V5     10k
 5:  R_R4        V3  V2     100M
 6:  C_C1        0  V6     1n
 7:  R_R3        V5  V6     0.001
 8:  R_R5        0  V3     10k
 9:  E_E1        0  V5  V2  V3  1000000000
10:  R_R6        V3  V4     1k
11:  V_V2        V4  0   1.01Vdc
12: .OP
13: .PRINT DC node voltage  V6
14: .END
(  V6)     .1000
```

Observe that the 1 nF capacitance is connected from node 6 to ground. In Sec. 1-9 we demonstrated that a capacitance behaves as an open-circuit to a constant voltage.[7] Thus, no current exists in the loop containing R3 and C1. This capacitive behavior is described in more detail in Chap. 7.

[7] $i_c = C\frac{dv_c}{dt}$ and for v_c = constant, $\frac{dv_c}{dt} = 0 = i_c$

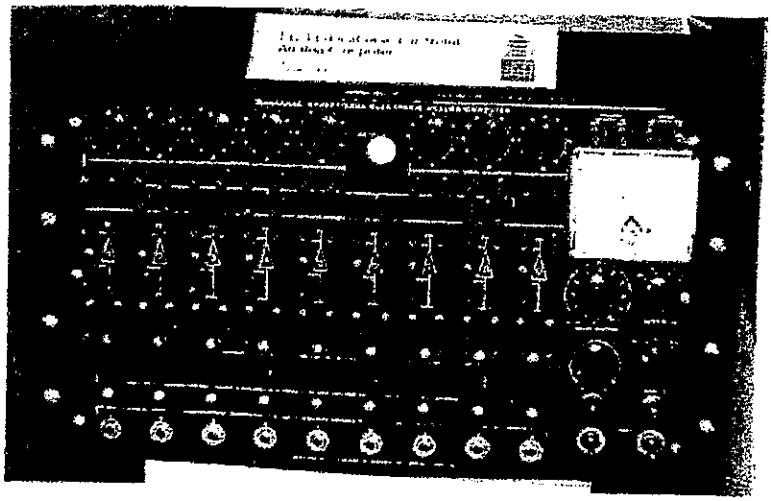


Fig. 4-1

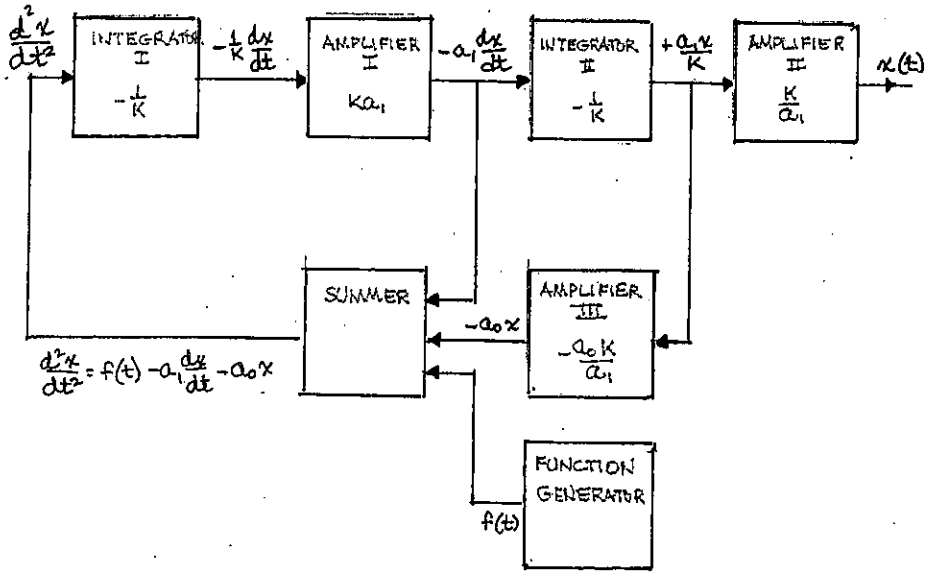
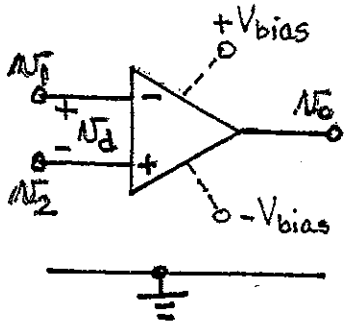
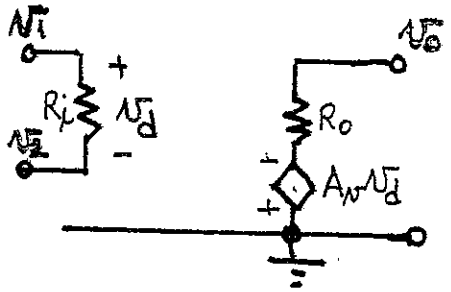

$\frac{d^2x}{dt^2}$
INTEGRATOR I
$-\frac{1}{K}$
$-\frac{1}{K}\frac{dx}{dt}$
AMPLIFIER I
Ka_1
$-a_1\frac{dx}{dt}$
INTEGRATOR II
$-\frac{1}{K}$
$+\frac{a_1x}{K}$
AMPLIFIER II
$\frac{K}{a_1}$
$x(t)$
SUMMER
AMPLIFIER III
$-\frac{a_0K}{a_1}$
$-a_0x$
$\frac{d^2x}{dt^2} = f(t) - a_1\frac{dx}{dt} - a_0x$
FUNCTION GENERATOR
$f(t)$

Fig 4-12



(a)



(b)

Fig 4-3

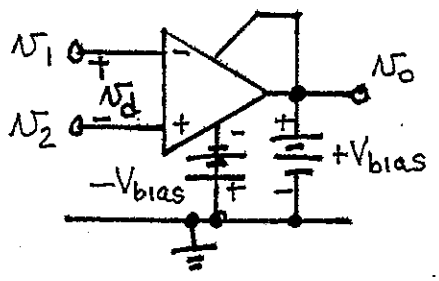


Fig 4-A

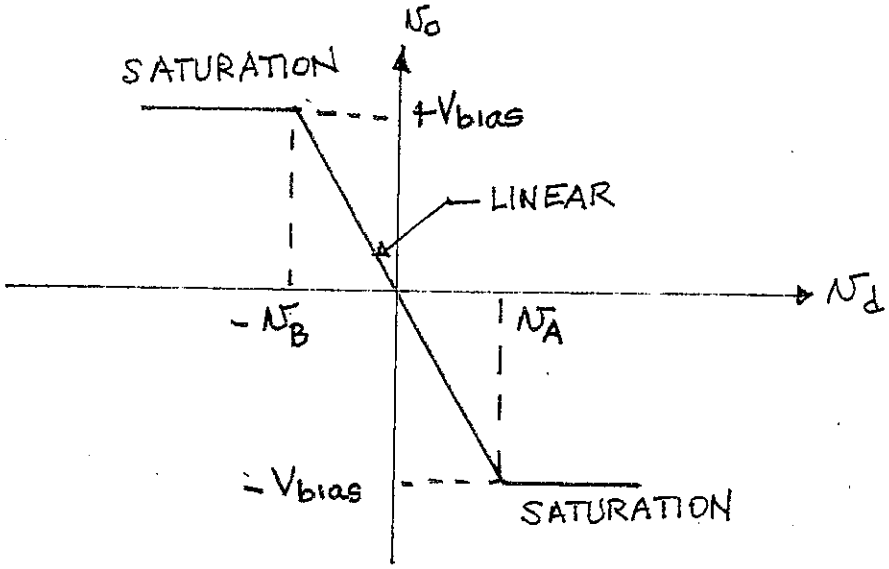


Fig 4-5

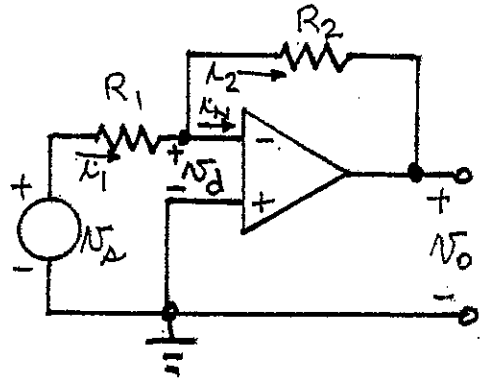


Fig 4-6

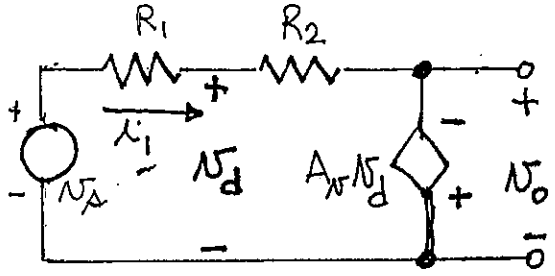
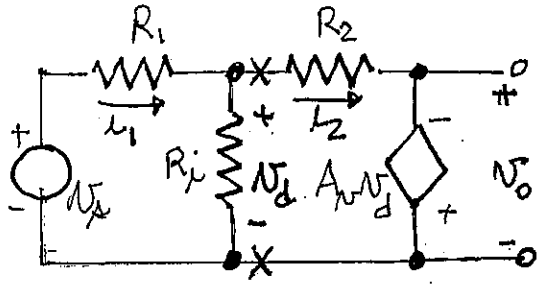


Fig. 4-7



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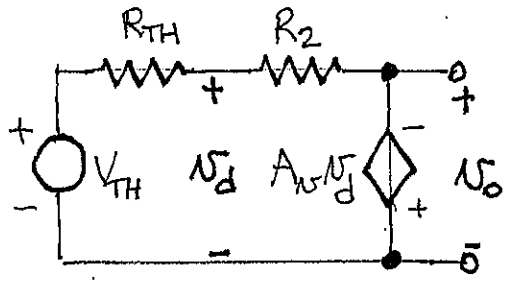
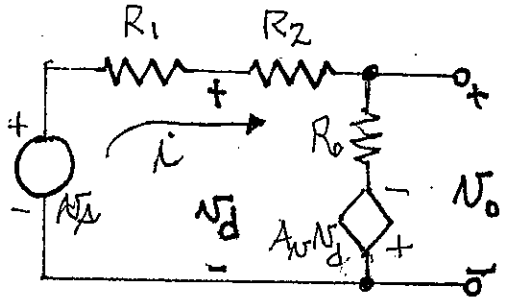
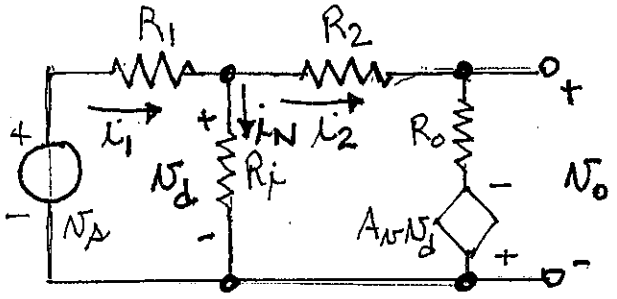


(b)

Fig 4-8



new
Fig. 4-7



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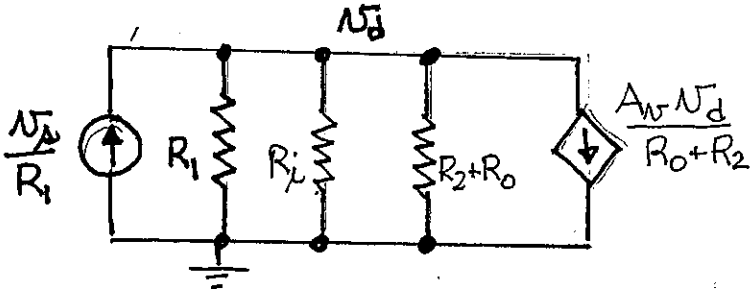
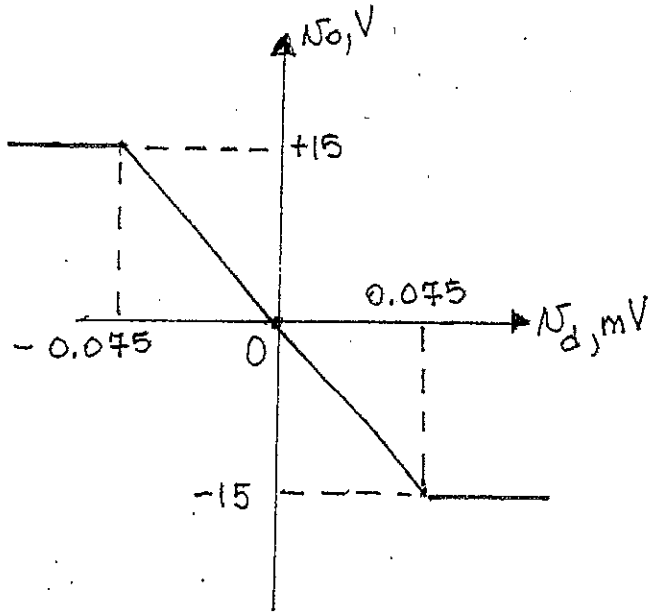
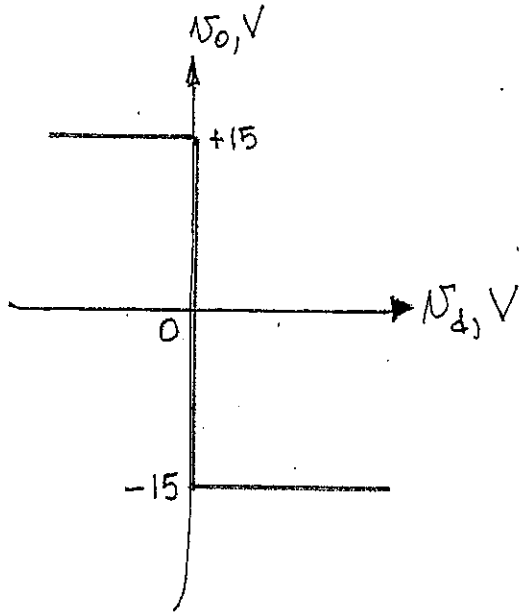


(b)

Fig. 4-10



(a)



(b)

Fig 4-91

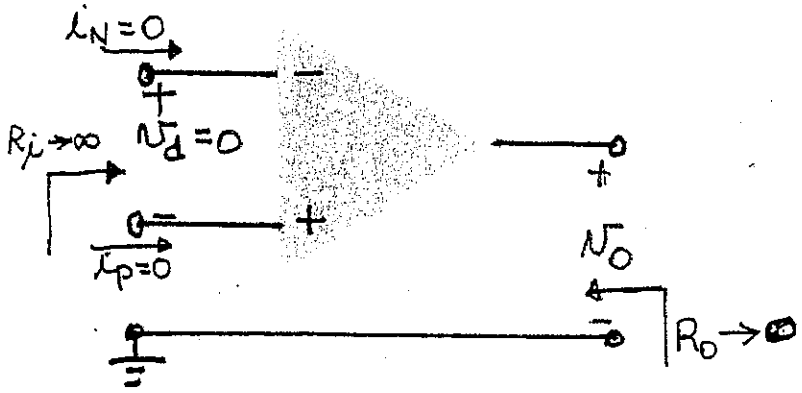


Fig 4-12

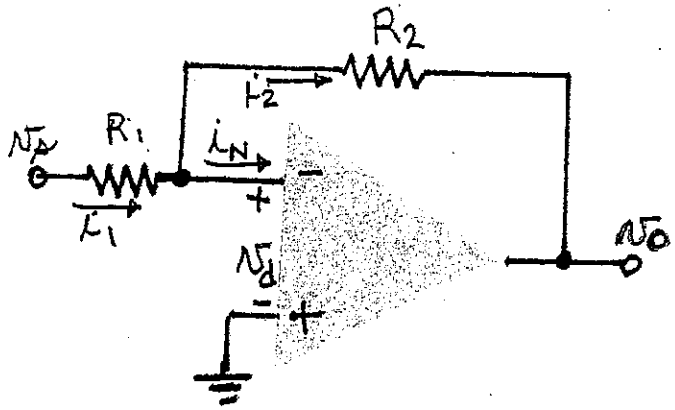


Fig. 4-8

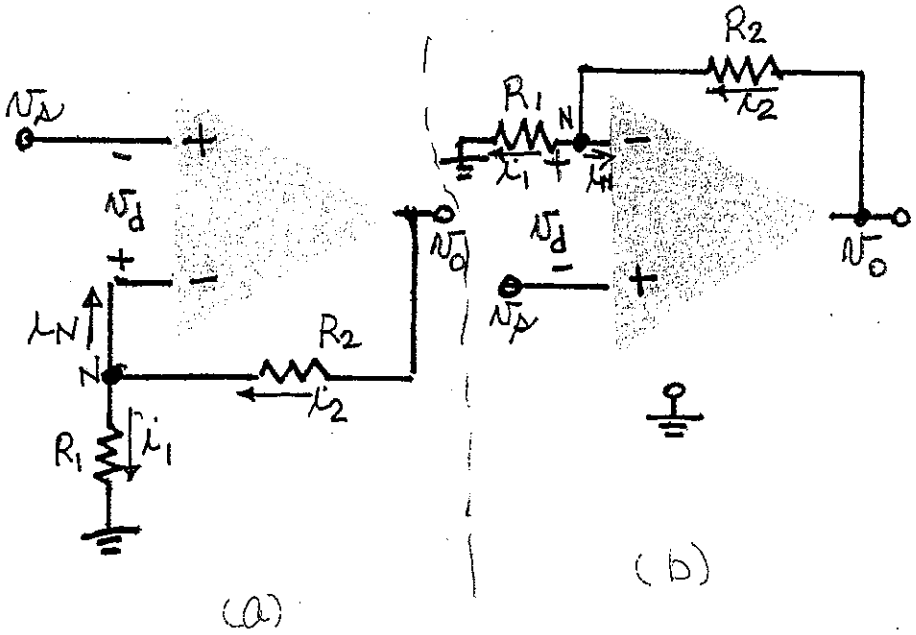


Fig 4-14

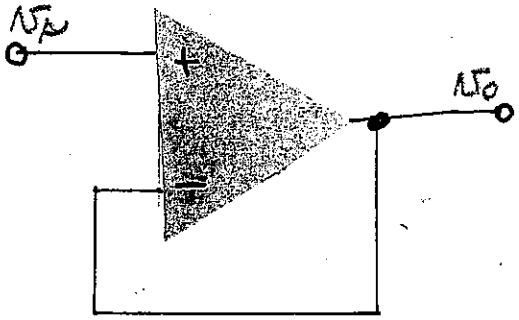


Fig. 4-15

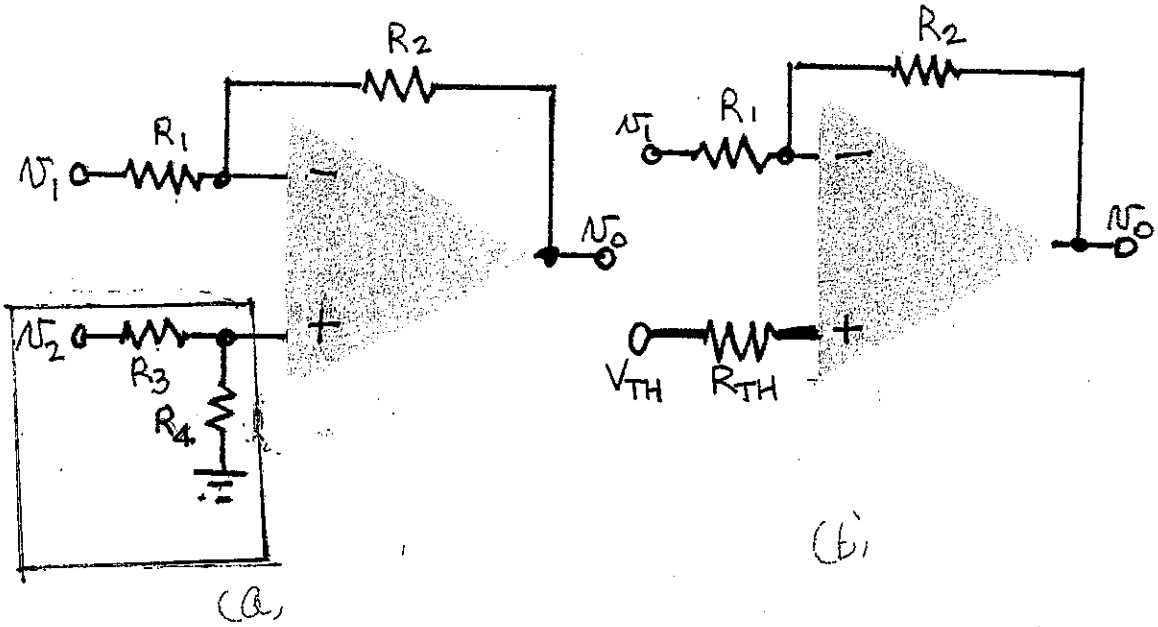
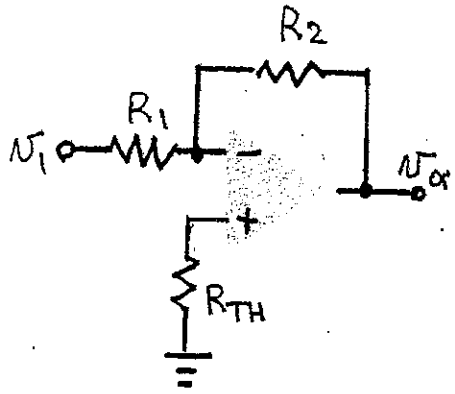


Fig 4-16



(a)

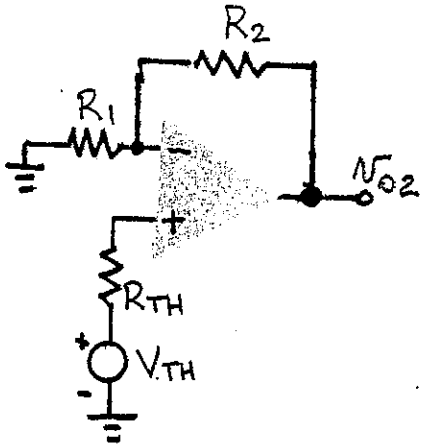


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Fig 4-17

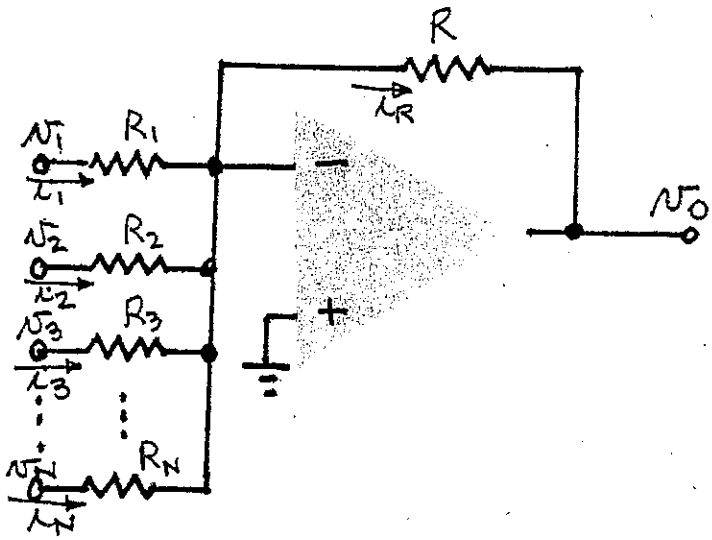


Fig 4-18

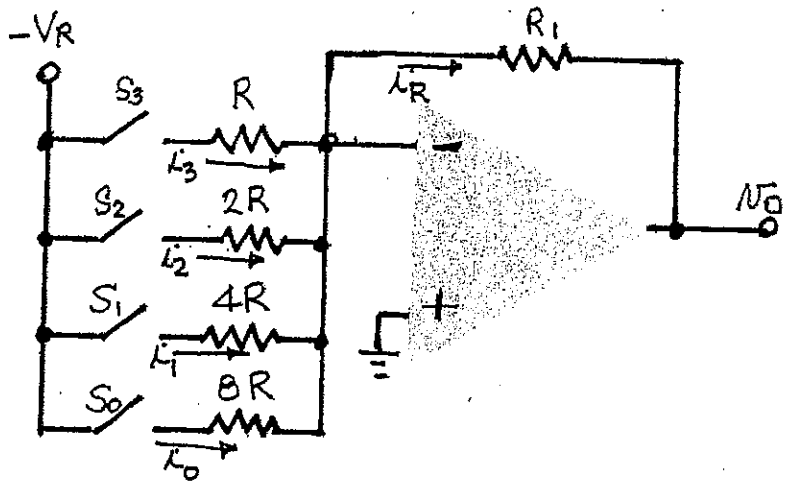


Fig 4-19

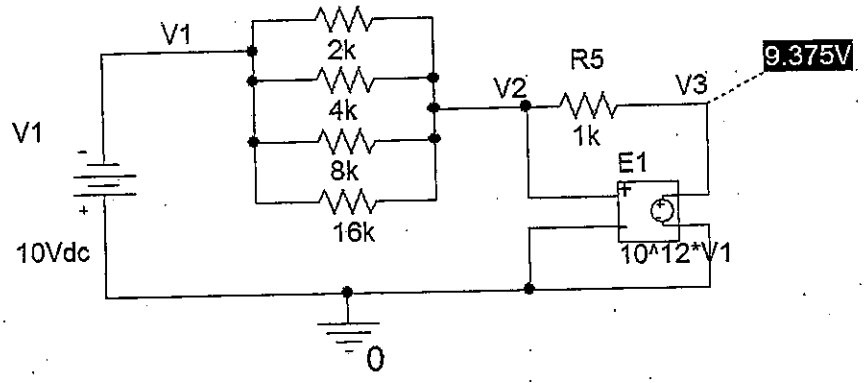


Fig 4-28

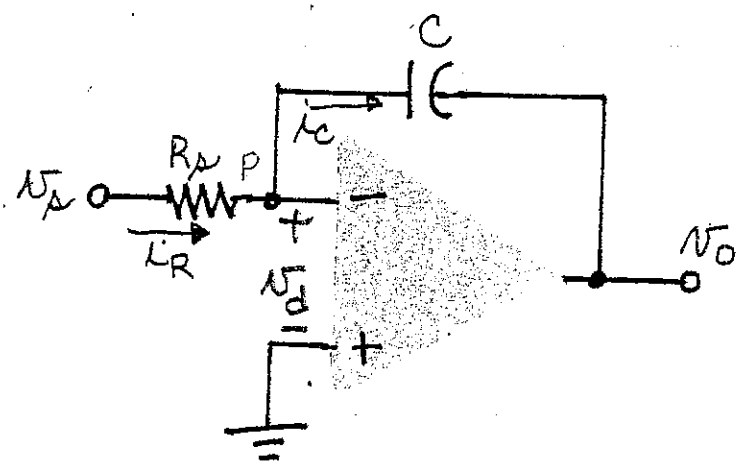
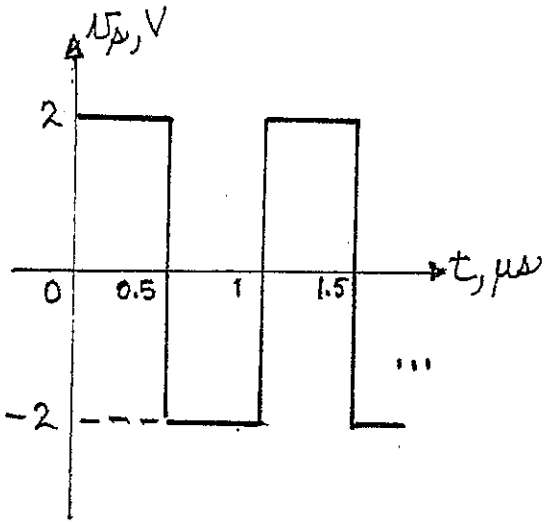


Fig 4-20



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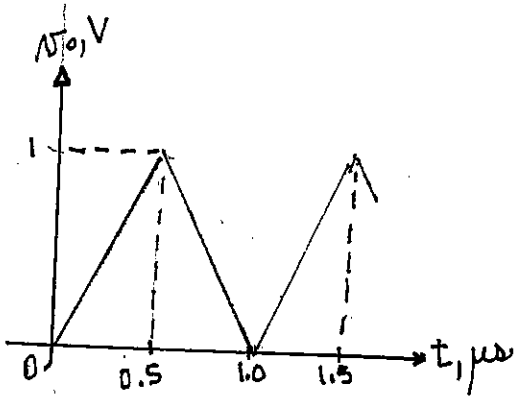

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Fig 4-23

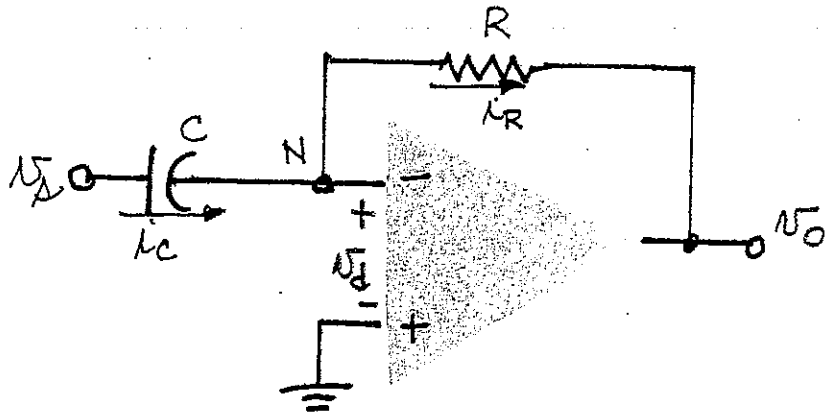
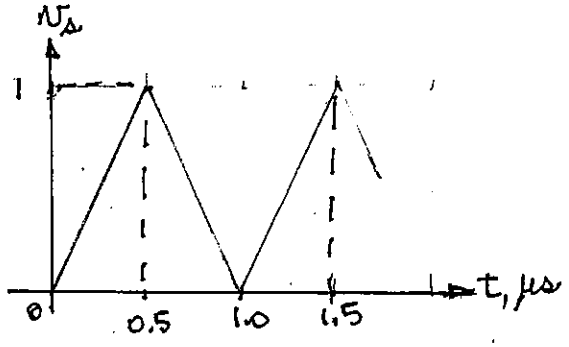


Fig 4-22



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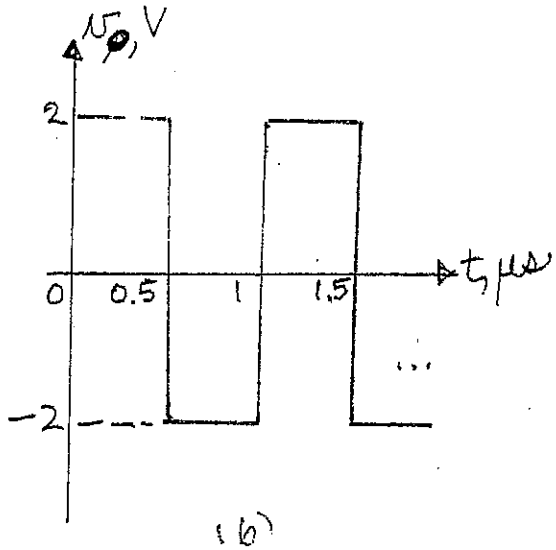

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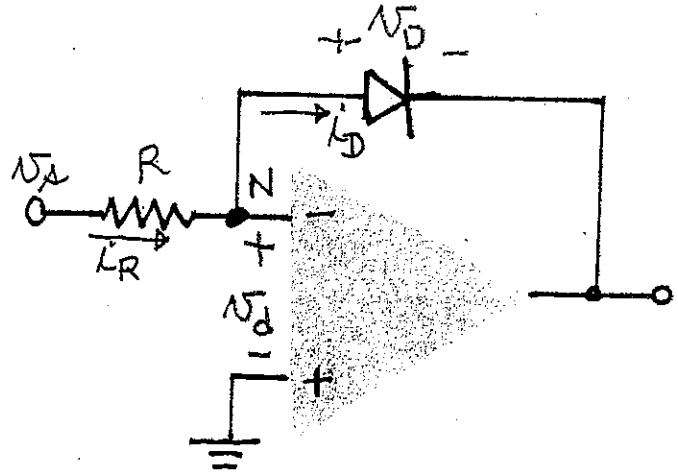
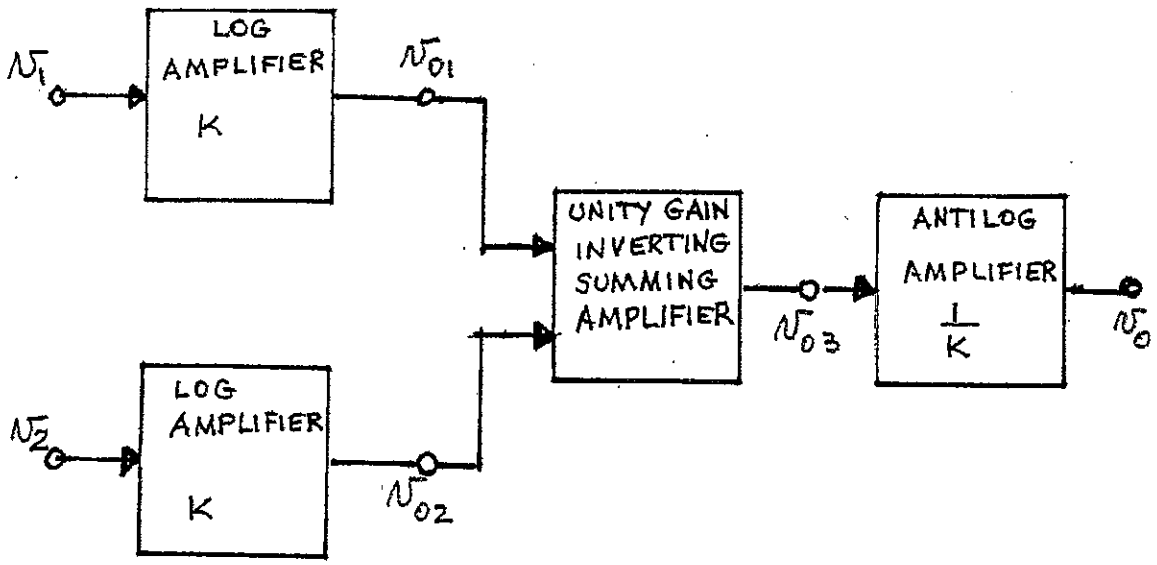


Fig 4-26


LOG
AMPLIFIER
K
V_1
V_{01}
LOG
AMPLIFIER
K
V_2
V_{02}
UNITY GAIN
INVERTING
SUMMING
AMPLIFIER
V_{03}
ANTILOG
AMPLIFIER
$\frac{1}{K}$
V_0

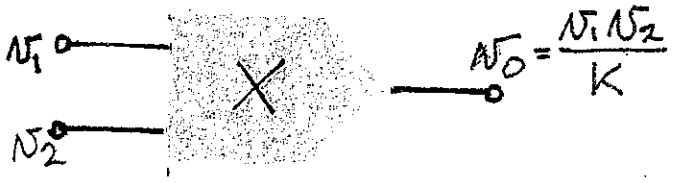
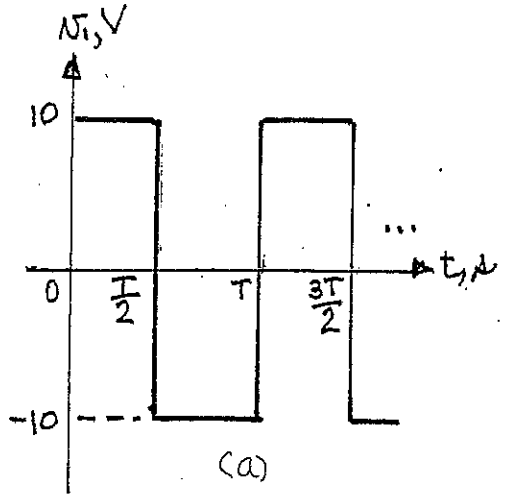
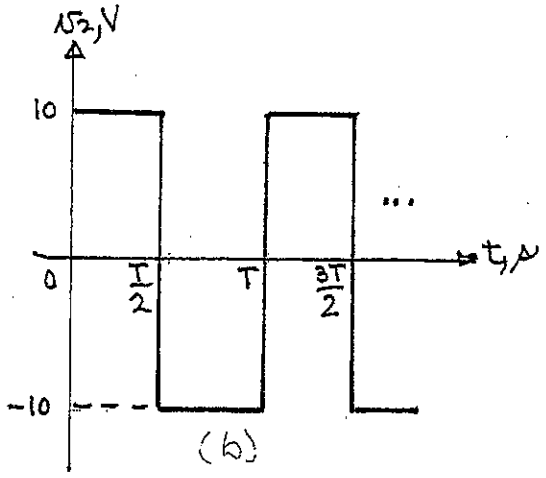
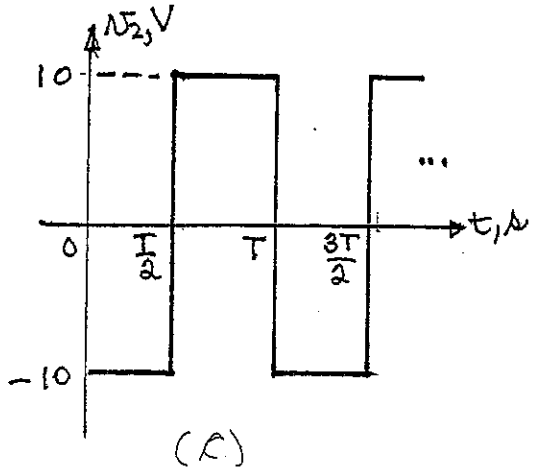


Fig 4-29


v1, V
10
-10
0
T/2
T
3T/2
t, s
(a)


v2, V
10
-10
0
T/2
T
3T/2
t, s
(b)


v2, V
10
-10
0
T/2
T
3T/2
t, s
(c)

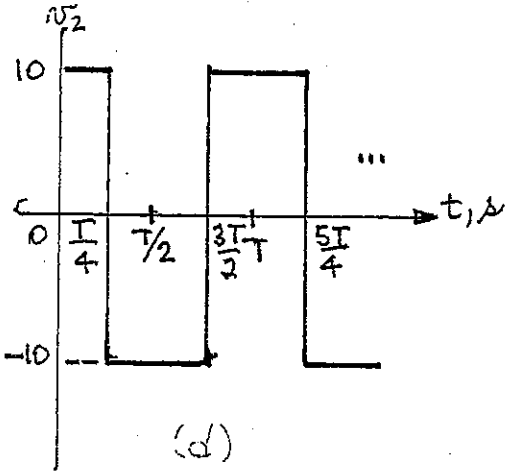
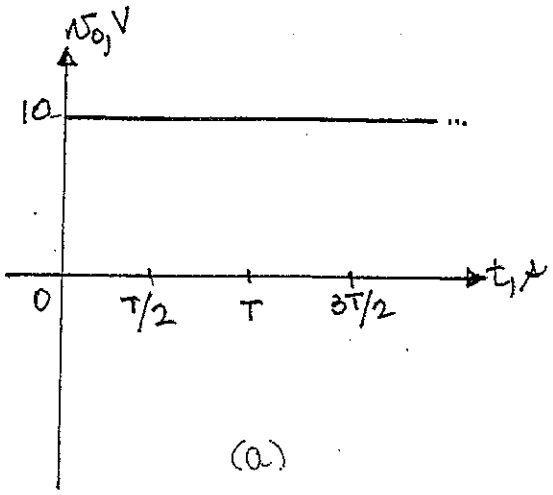
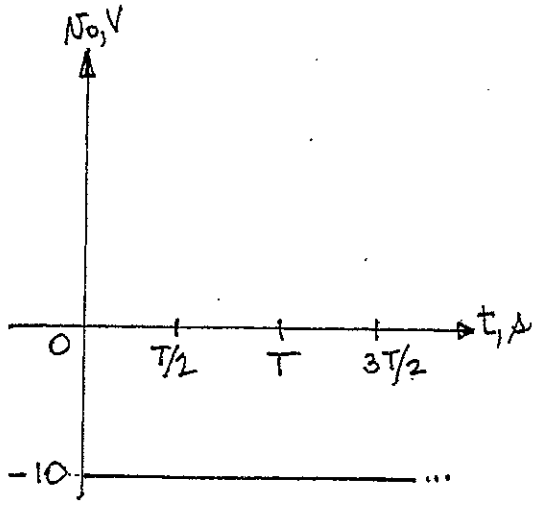

v2
10
-10
0
T/4
T/2
3T/4
T
5T/4
t, s
(d)

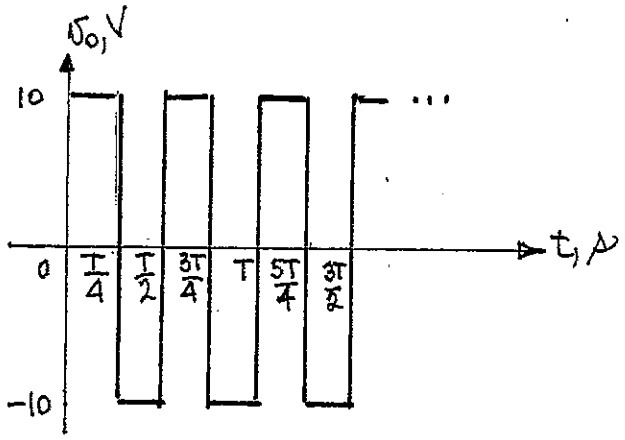
Fig 4-28


v_o, V
10
0
T/2
T
3T/2
t, s

(a)


v_o, V
0
T/2
T
3T/2
t, s
-10

(b)


v_o, V
10
0
T/4
T/2
3T/4
T
5T/4
3T/2
t, s
-10

(c)

Fig 4-34

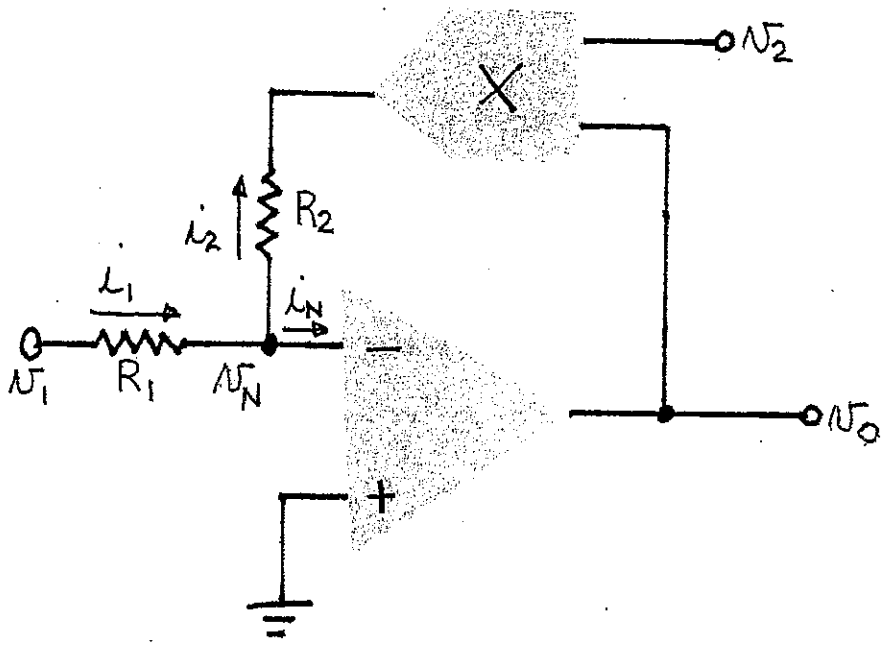


Fig 4-38

Fig 4-31

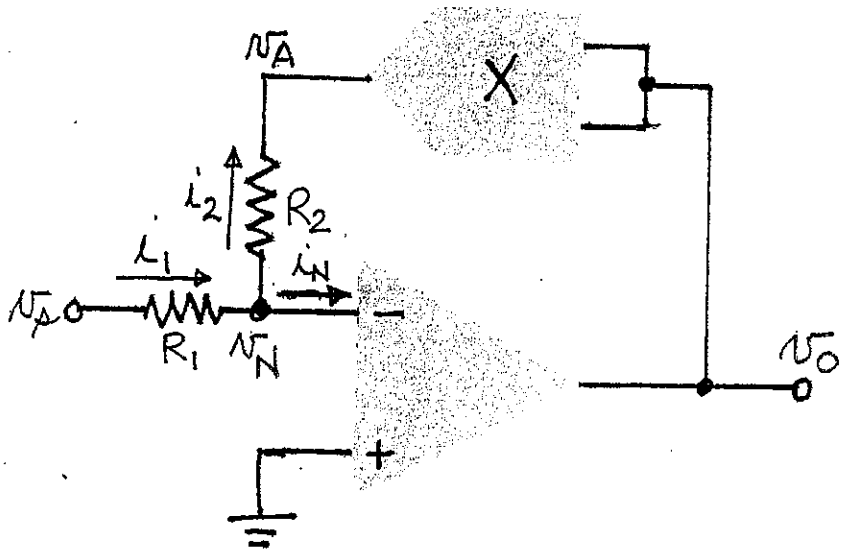


Fig 4-32

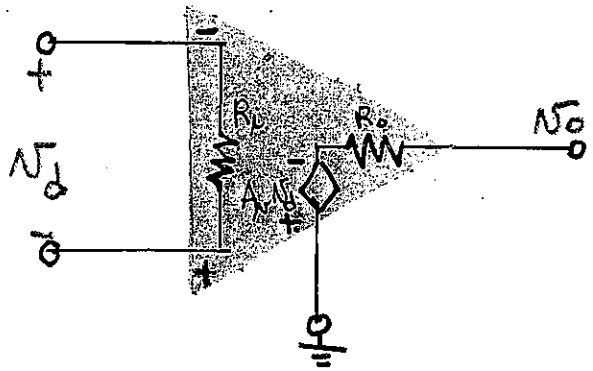
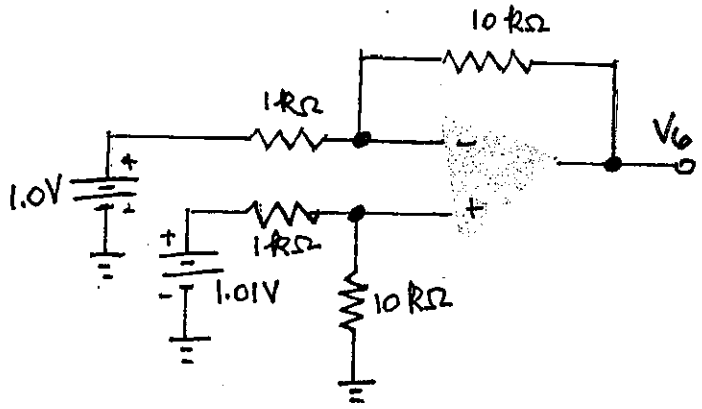
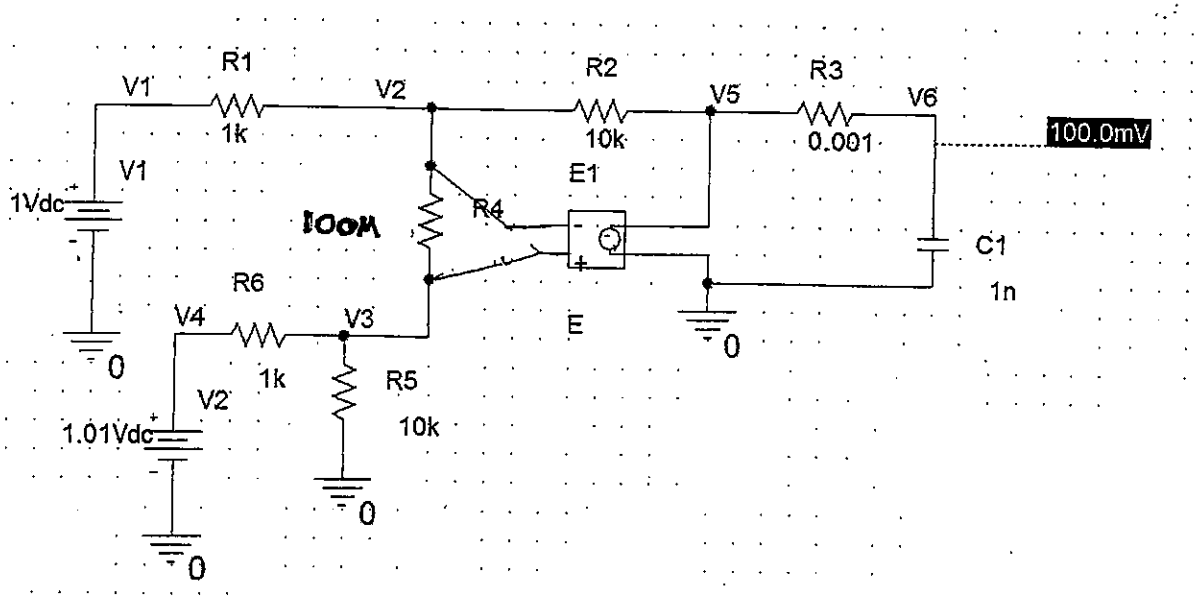


Fig. 4-35


10 kΩ
1kΩ
V6
1.0V
1kΩ
1.01V
10 kΩ

(a)


R1
V1
V2
R2
V5
R3
V6
1k
10k
0.001
100.0mV
V1
1Vdc
E1
100M
R4
C1
1n
R6
V4
V3
E
0
1k
R5
V2
10k
1.01Vdc
0
0
0

(b)

Fig 4-36