Texts


Course Objectives
1. Review the fundamental system elements in a computer system
2. Develop a better understanding of the hardware-software interface
3. Demonstrate quantitative methods to evaluate different design implementations
4. Provide an in-depth study of the critical system elements including, the processor pipeline, memory hierarchy, bus interconnects and the I/O subsystem

Homeworks
During the quarter there will be homework problem sets assigned bi-weekly. Many of the problems will be taken from the problem sets appearing at the end of each chapter in the H&P course text.

Paper Review
During the quarter there will be a set of papers provided that should build upon the principles presented in the textbook. You are responsible for all of the material contained in these papers. All of these papers will be available on the ECE3391/CA714 webpage in either postscript and/or pdf formats. From these papers you will be asked to write a paper review. The review should be at least 5 pages in length, single spaced, and typewritten. The review should be technical in nature. It should not merely summarize the paper. Instead it should critique the paper, drawing on one or a number of the references listed in the papers as a comparison.

You should address the following questions in your review:
1. What is the problem begin addressed?
2. What methods are used to evaluate this problem and/or solution?
3. Are the methods used validate and proper?
4. What conclusions can we draw from the results presented?
5. How do results in the cited references compare with those presented in this paper?
6. Is this paper well written?

Exams
There will be a final exam. The exam will be open book and open notes.

Project
There will be project assigned. See the webpage for details.

Grading
Homeworks - 40%
Paper Review - 10%
Project - 25%
Final - 25%
Schedule (subject to change)

Week 1: Chapters 1 and 2 - History, Performance and Cost, Instruction Sets
Week 2: Chapters 2 and 3 - Instruction Sets, Register Sets, Operands, Addressing, DLX
Week 3: Chapter 3 - Pipelined DLX, Hazards
Week 4: Chapter 4 - Instruction Level Parallelism, Compilation, Dynamic Scheduling
Week 5: Chapter 4 - Dynamic Scheduling, Limits on ILP, Prediction, Predication
Week 6: Chapters 4 and 5 - VLIW, DRAM, SRAM, Main Memory, Caches
Week 7: Chapter 5 - Prefetching, Code and Data Layout, Virtual Memory
Week 8: Chapter 6 - I/O, Busses, RAID, Network Attached Storage
Week 9: (From H&P 3rd edition) Embedded Processors, DSPs
Week 10: Chapters 7 and 8 - Interconnects, Multiprocessors, Cache Coherency, Memory Consistency
Week 11: Final Exam